

# MS-7C26

Version : 1.0

## CPU :

**AMD AM4**

## System Chipset :

**AMD PROMONTORY**

## On Board Chipset :

**Intersil 6377HRZ 6Phase**

**Gigabit LAN -- RTL8111GN/RTL8111EPV**

**HDA Codec -- Realtek ALC662VD**

**Super I/O ---IT8738E**

**SPI Flash 256Mb**

## Main Memory :

**2 Channel DDR 4 \* 4 (Max 64GB)**

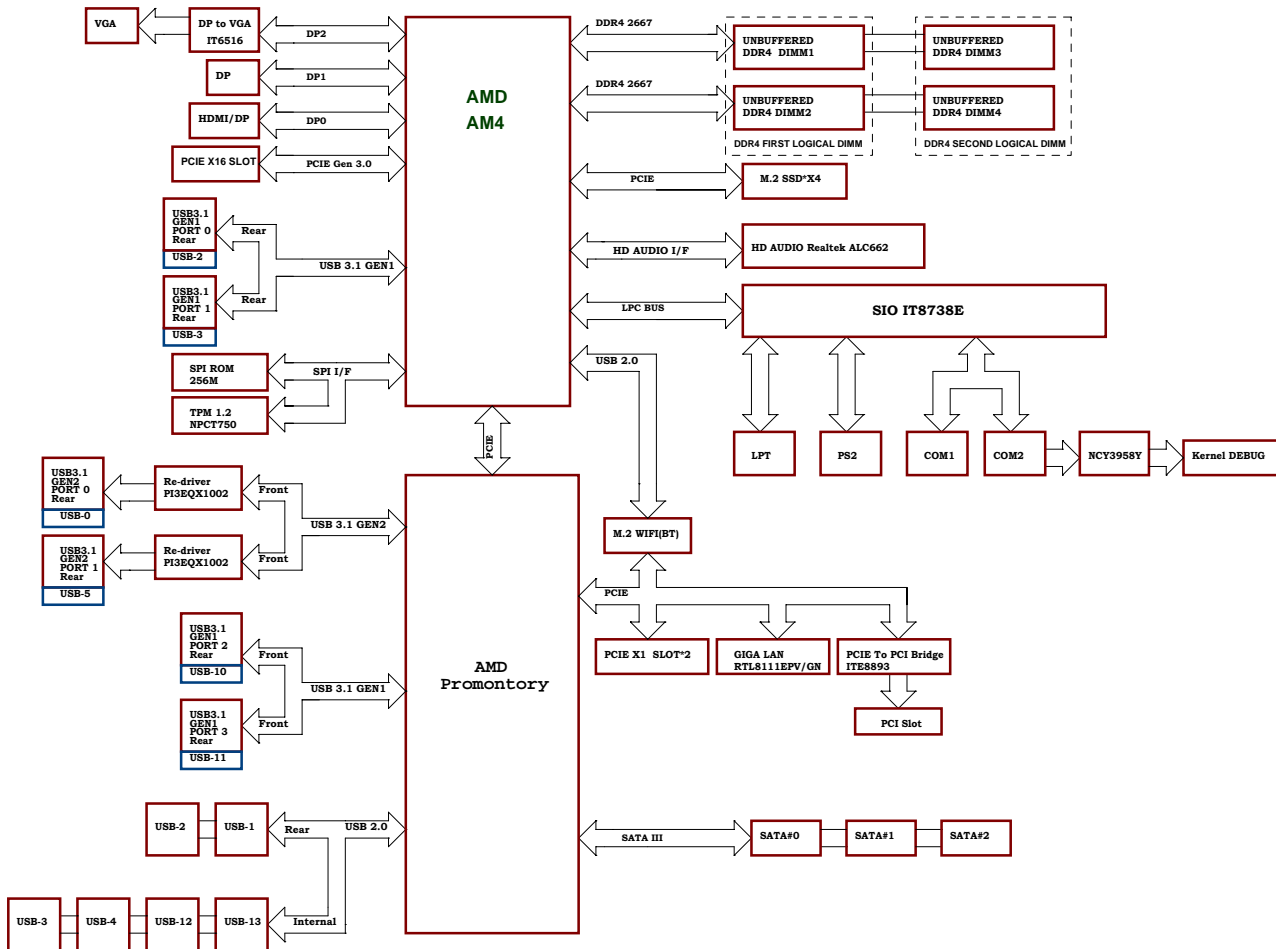
## Expansion Slot :

**PCI Express x16 Slot \* 1**

**PCI Express x1 Slot \* 2**

**PCI Slot \* 1**

# lenovo



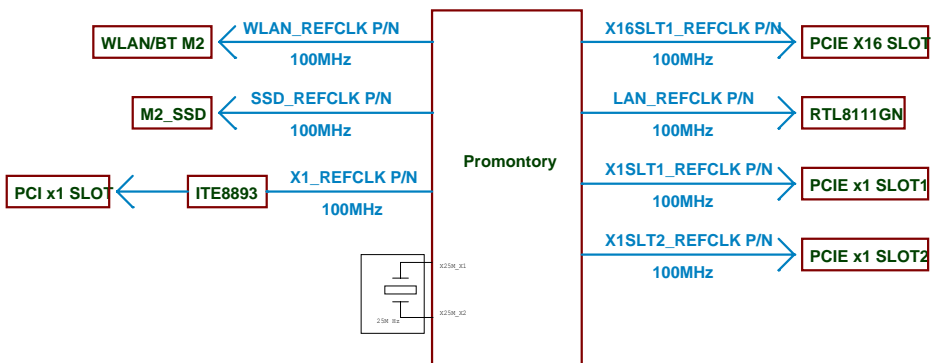
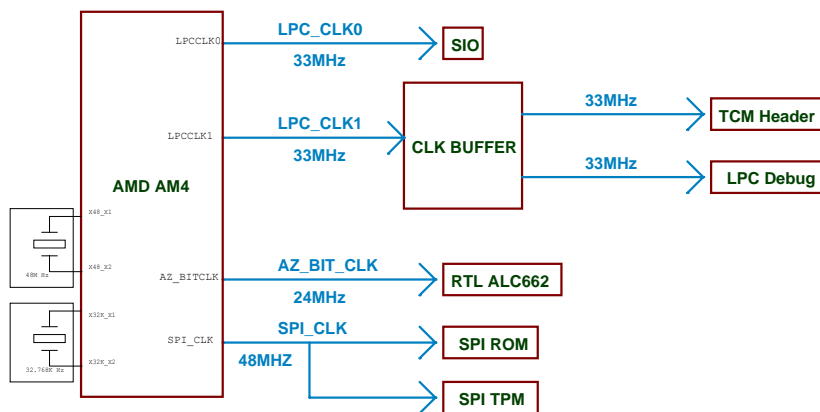
Slot Sequence:

PCIE X16

PCIE X1

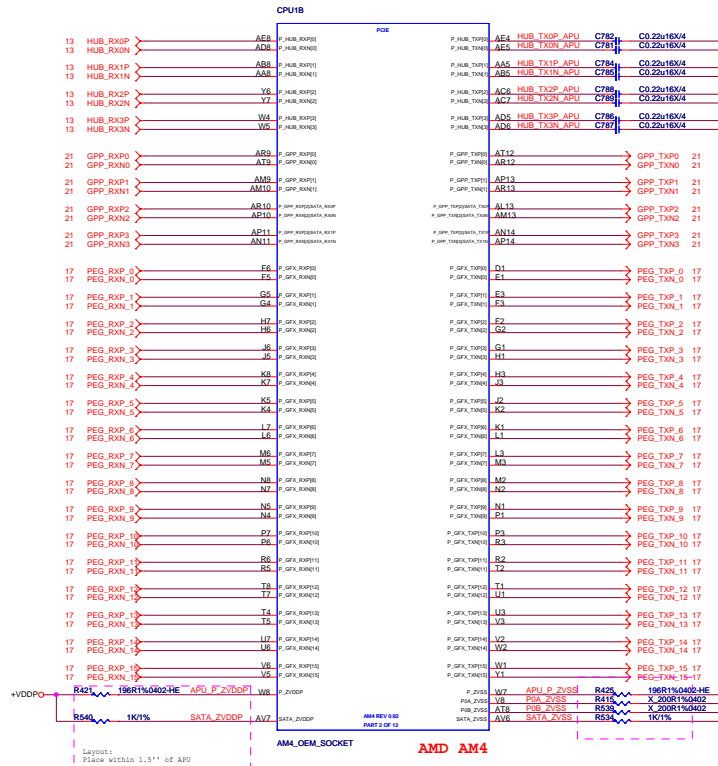
PCIE X1

PCI

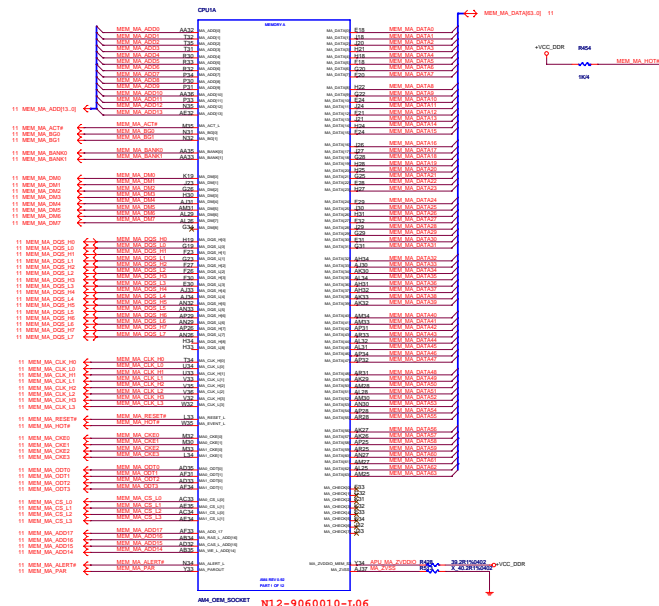


**AM4 PCIE I/F**

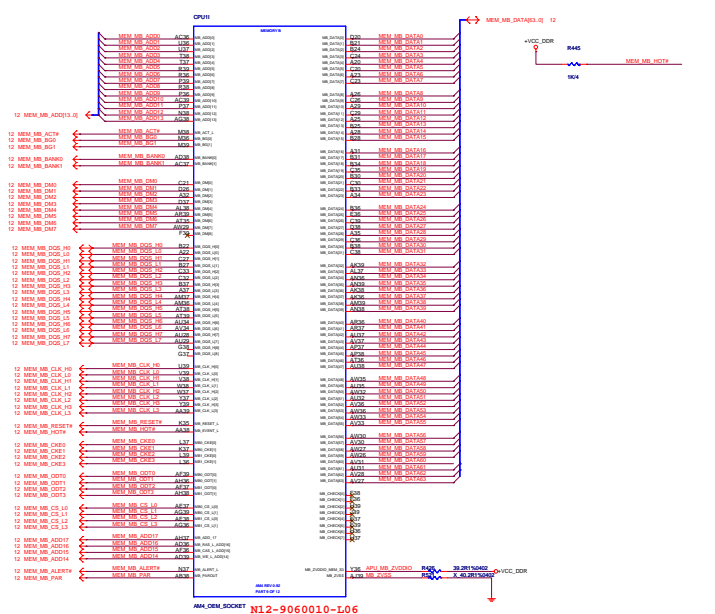
PCIe 3.0  
Allowable Range: 176 to 265 nF  
Recommended Value: 220 nF

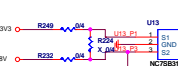
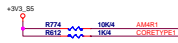
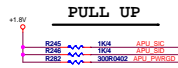


AM4 DDR4 I/F(A)



AM4 DDR4 I/F(B)



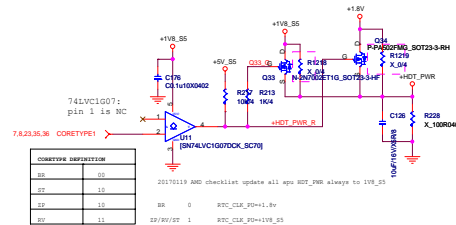
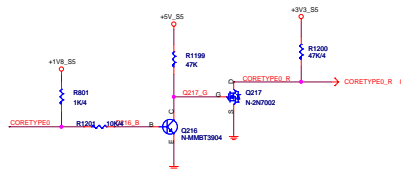
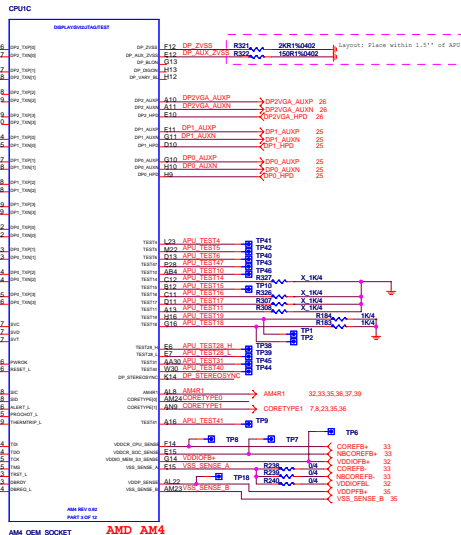
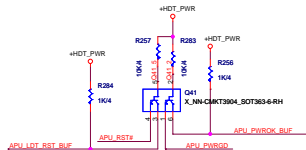


	CORETYPE 1	Function	FW4
Type 0	0	S2 Connected to D	Pull high to +1.8V
Type 2	1	S1 Connected to D	Pull high to +VCCIV3
Type 3	1	S1 Connected to D	Pull high to +VCCIV3

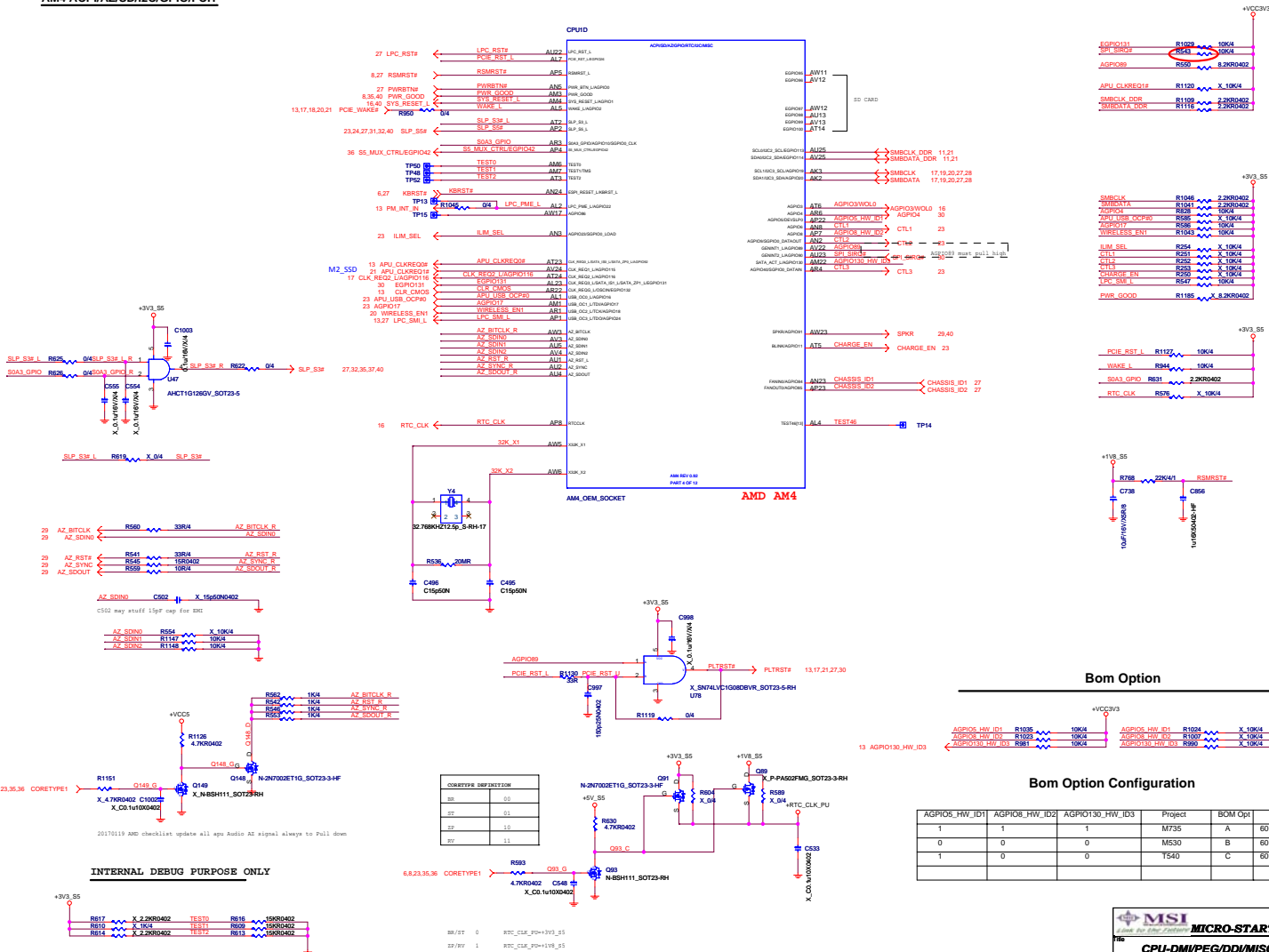
Pinout diagram for the N31-2100170-S88 connector. The diagram shows a 20-pin connector with pins numbered 1 to 20. The pins are color-coded: pins 1-10 are blue, pins 11-15 are green, and pins 16-20 are red. The pinout is as follows:

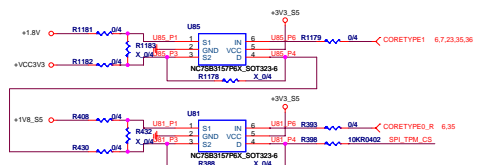
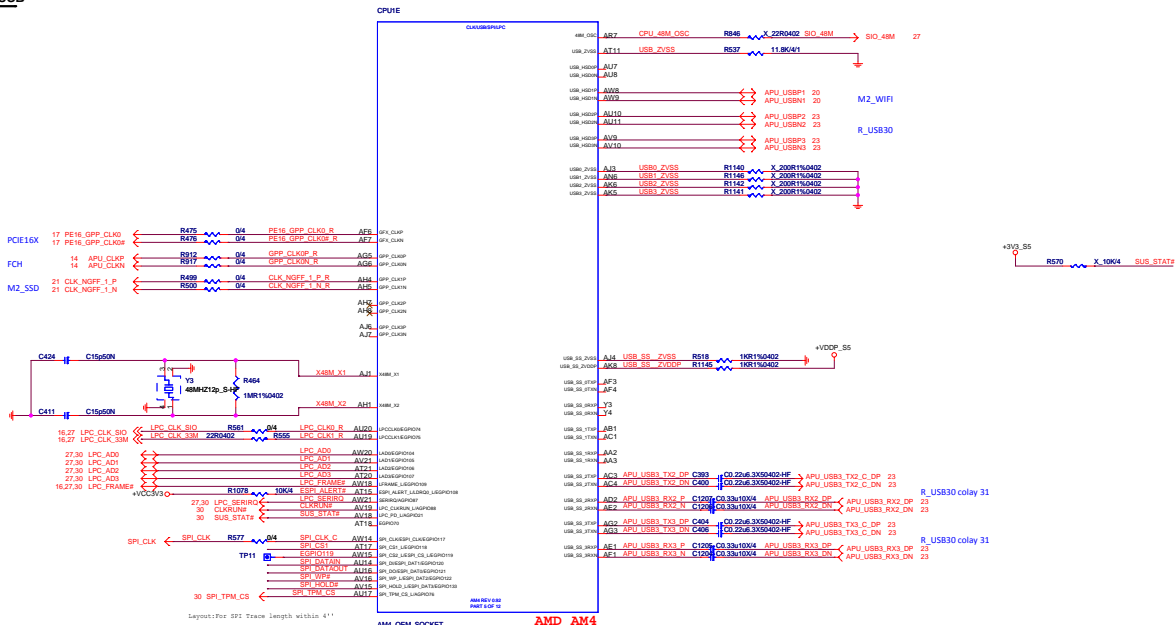
Pin	Signal
1	CPU_VDDIO
2	CPU_TCK
3	GND
4	CPU_TMS
5	CPU_RST
6	CPU_TDO
7	GND
8	CPU_TDI
9	CPU_PWROK_BUF
10	CPU_PWROK_BUF
11	CPU_TRST_L
12	CPU_DRDY0
13	CPU_DRDY2
14	CPU_DRDY0
15	CPU_DRDY0
16	CPU_DRDY0
17	GND
18	CPU_PILTEST0
19	CPU_VDDIO
20	CPU_PILTEST1

The connector is labeled 'XPC1006A1.27PITCH\_0000' and 'N31-2100170-S88'.

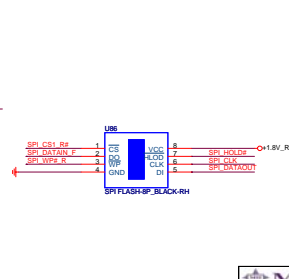
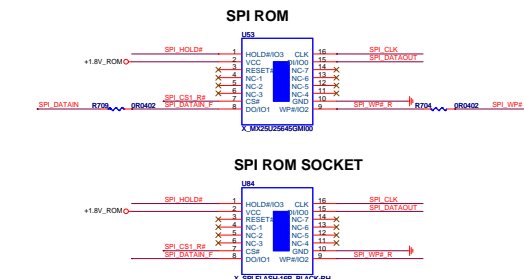
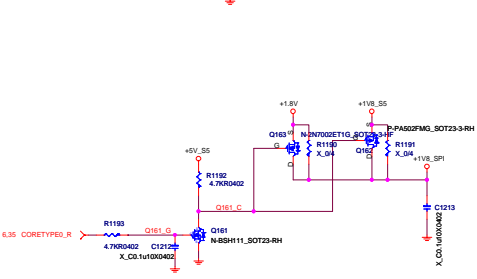
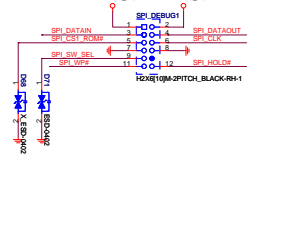
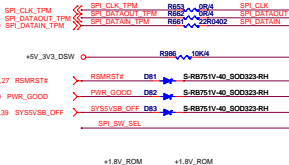
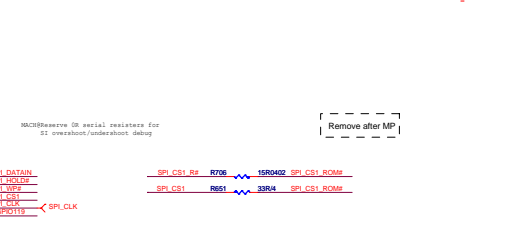
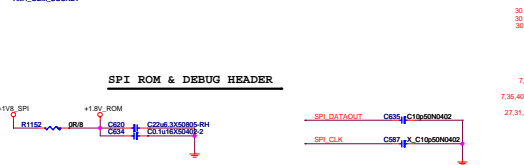
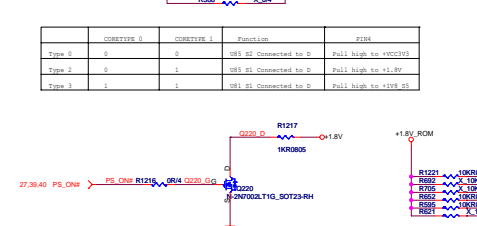
[illegible]

CORETYPE to Model Number Mapping			
CORETYPE1	CORETYPES	Family/Model Numbers	ARM Processor Type
0	0	Family 15h/Models 60h-6Fh	Type 0 Bristol
0	1	Reserved	Type 1
1	0	Family 17h/Models 50h-5Fh	Type 2 Summit
1	1	Family 17h/Models 15h-1Fh	Type 3 Rovan



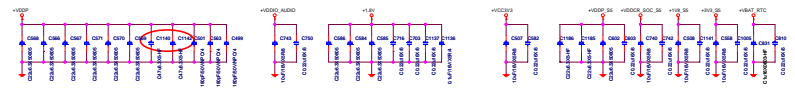
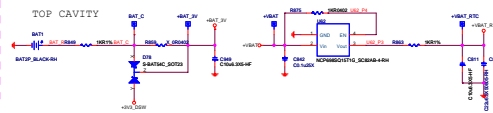
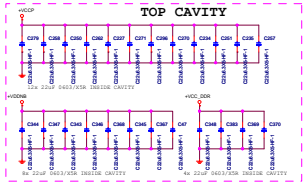
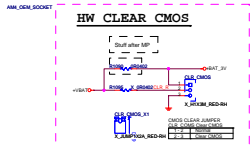
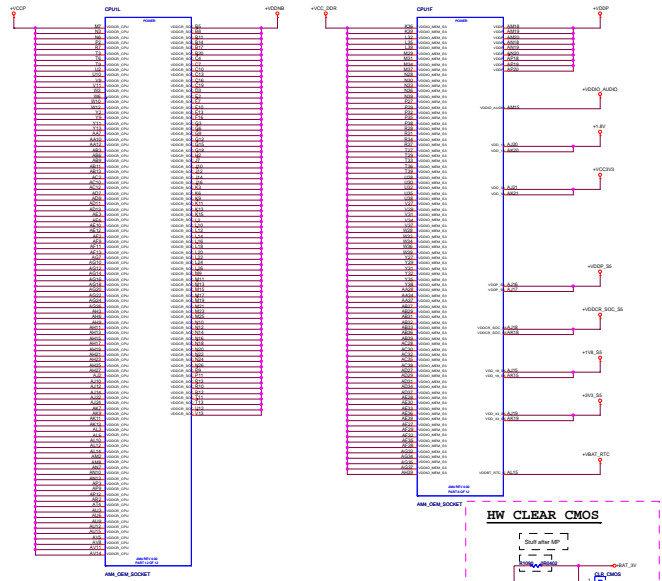


	CORETYPE 0	CORETYPE 1	Function	PIN4
Type 0	0	0	W5 S2 Connected to D	Pull high to +VCCV3
Type 2	0	1	W5 S1 Connected to D	Pull high to +1.8V
Type 3	1	1	W5 S1 Connected to D	Pull high to +1.8V

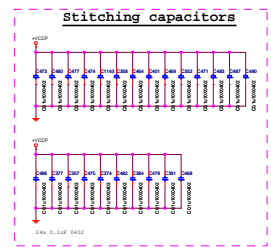




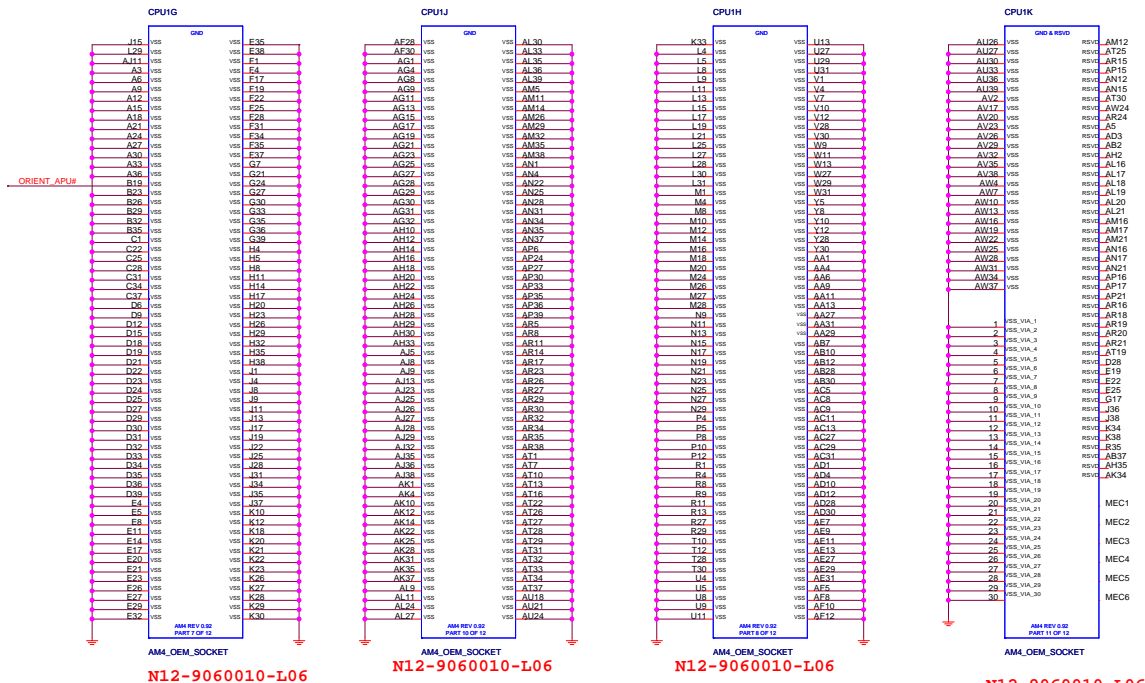
# AMA POWER

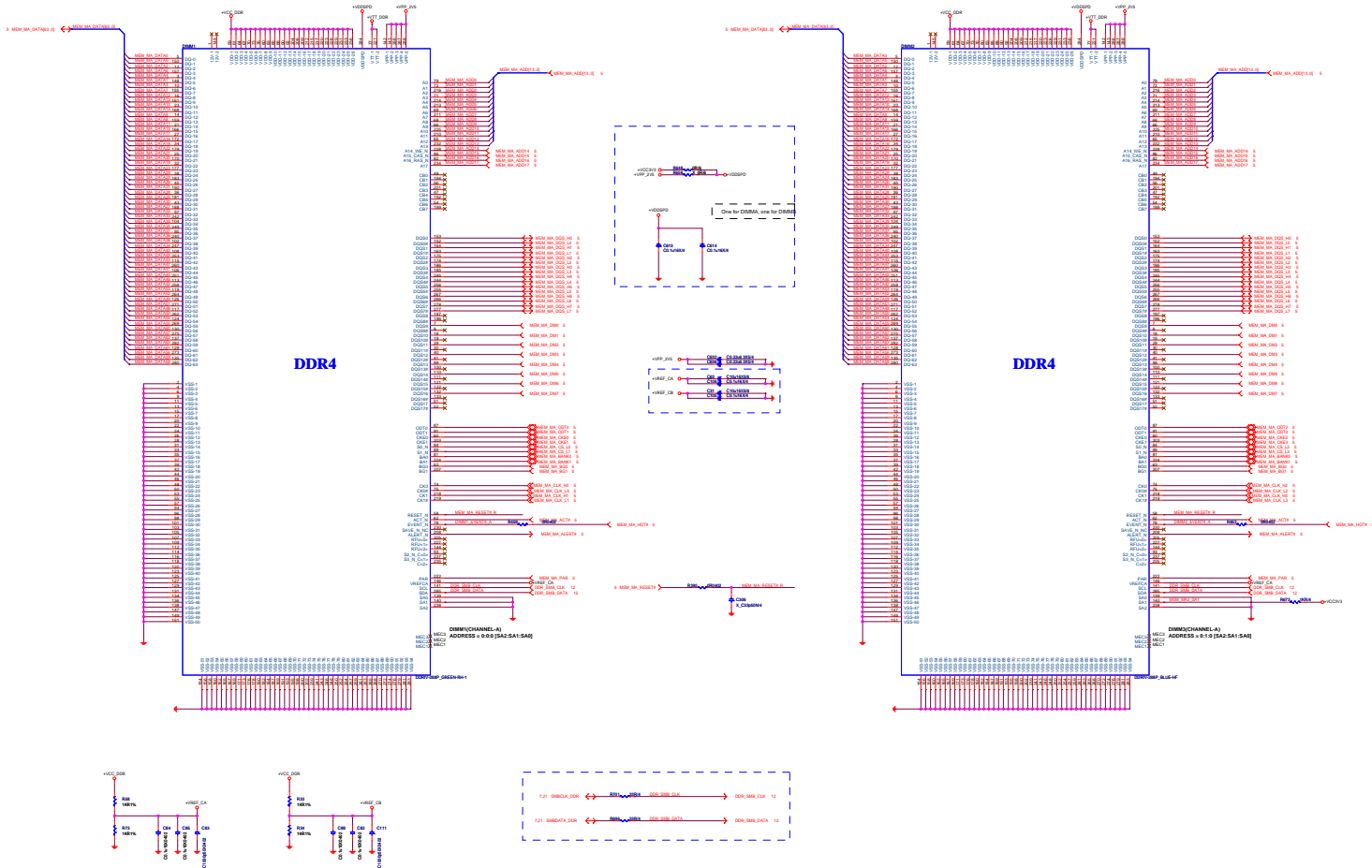


## BOTTOM SIDE DECOUPLING



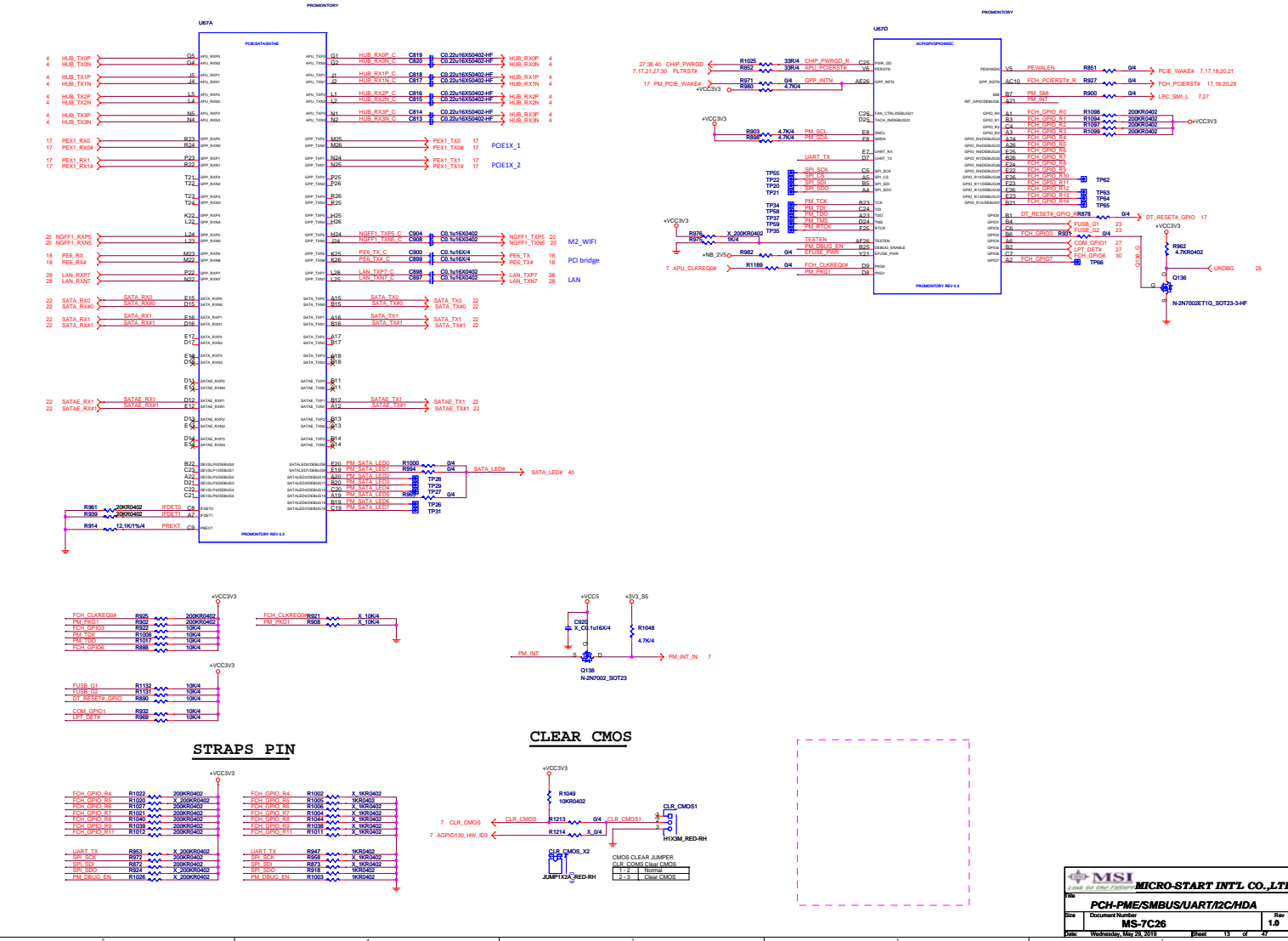
# AM4 GND



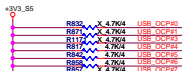




PROMONTORY PCIe/SATA/GPIO

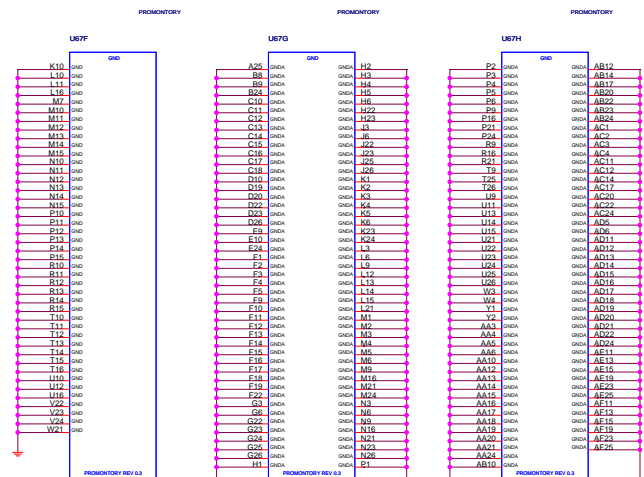
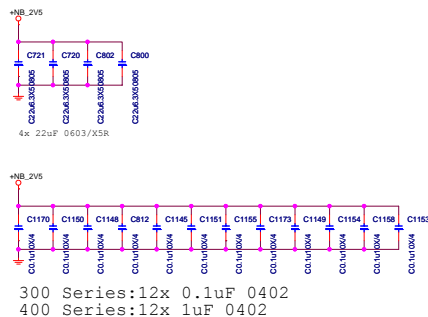
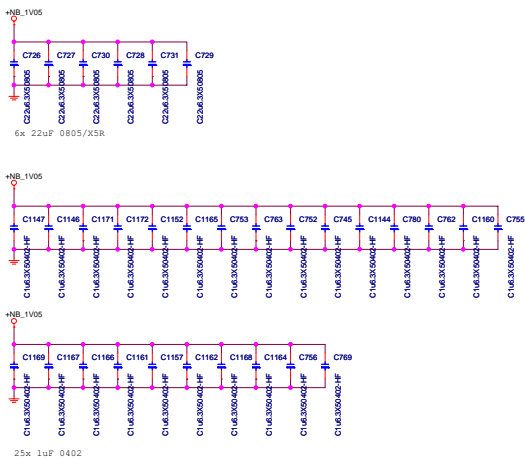
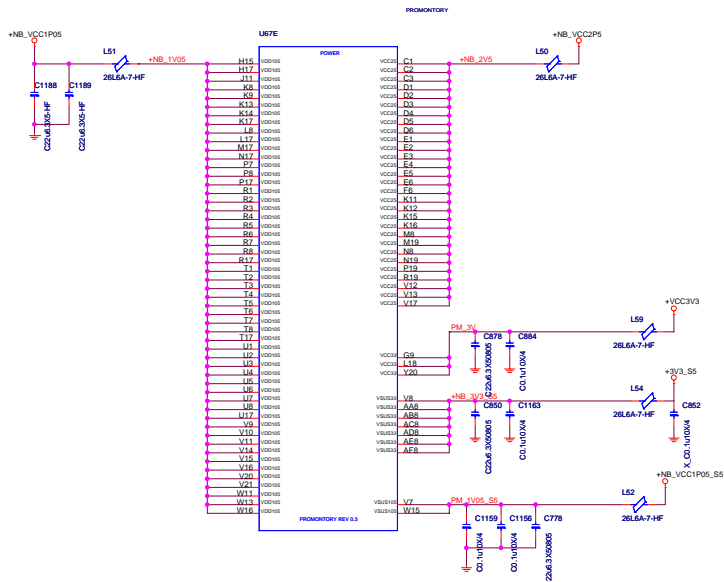


## PROMONTORY USB/CLOCK

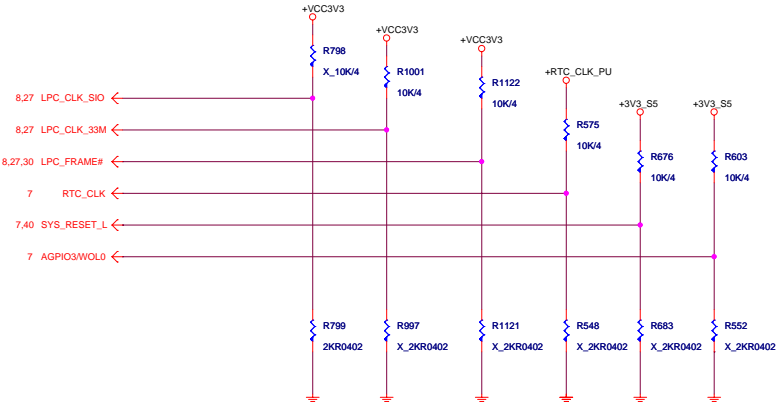


**B01-21807K5-AX8**

## PROMONTORY POWER



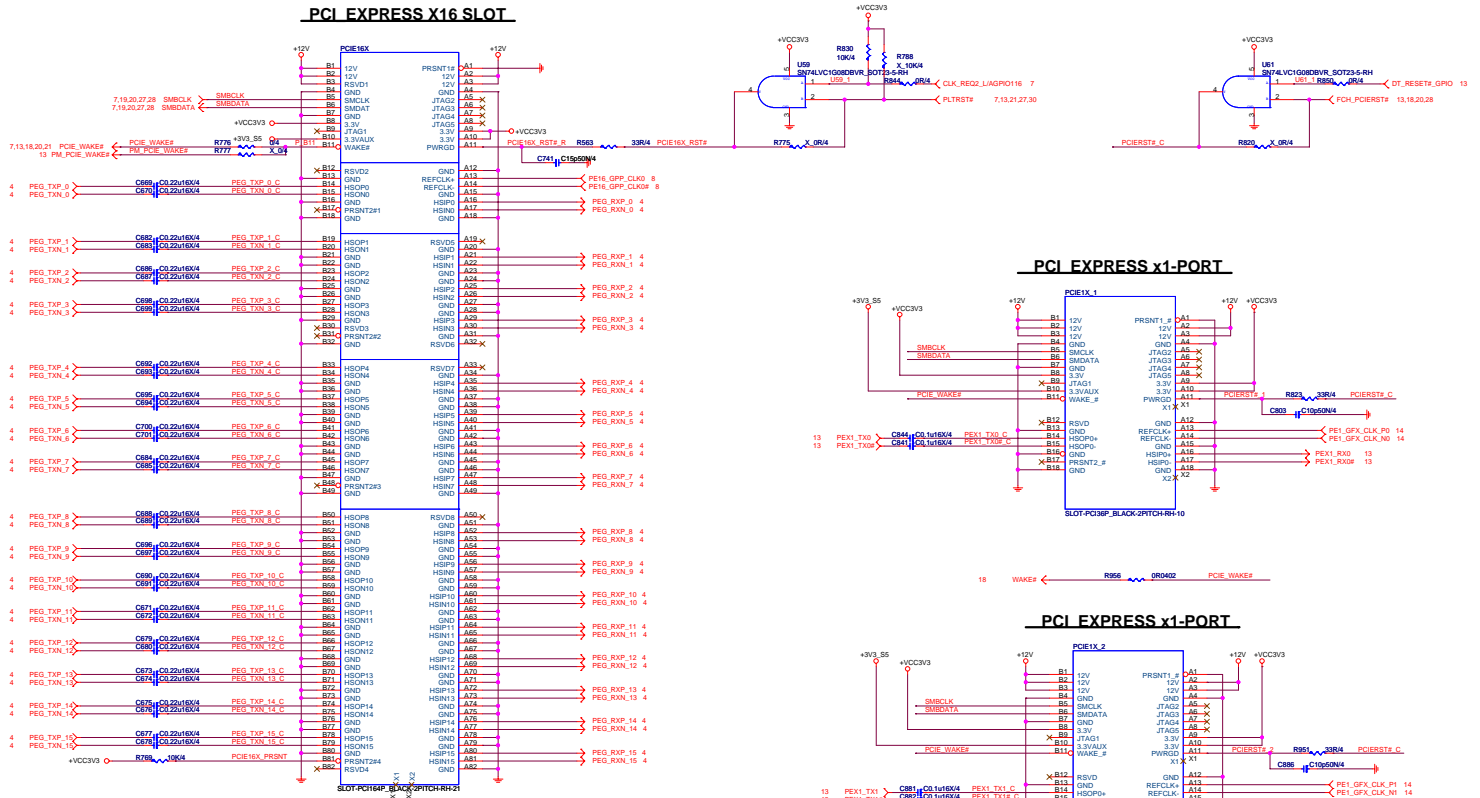
REQUIRED STRAPS

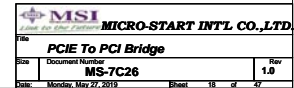


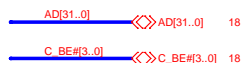
	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI CLK (ZP)
FULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board. (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)
FULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic	Coin battery is not on board.	LPC ROM	short reset mode	Use 100Mhz PCIE clock as reference clock and generate internal clocks only
C2/ST DIE ONLY						ZP DIE ONLY	




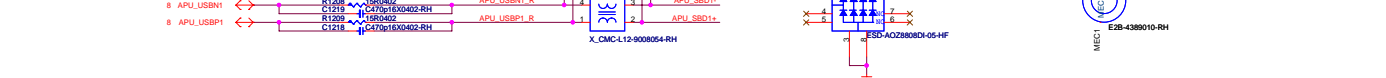
## PCI EXPRESS X16 SLOT

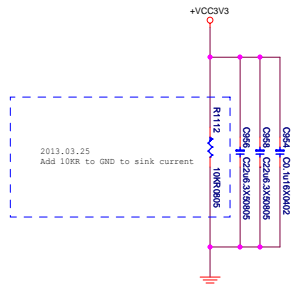


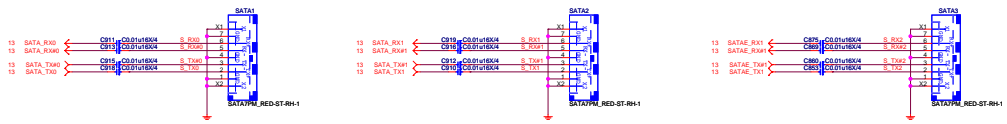




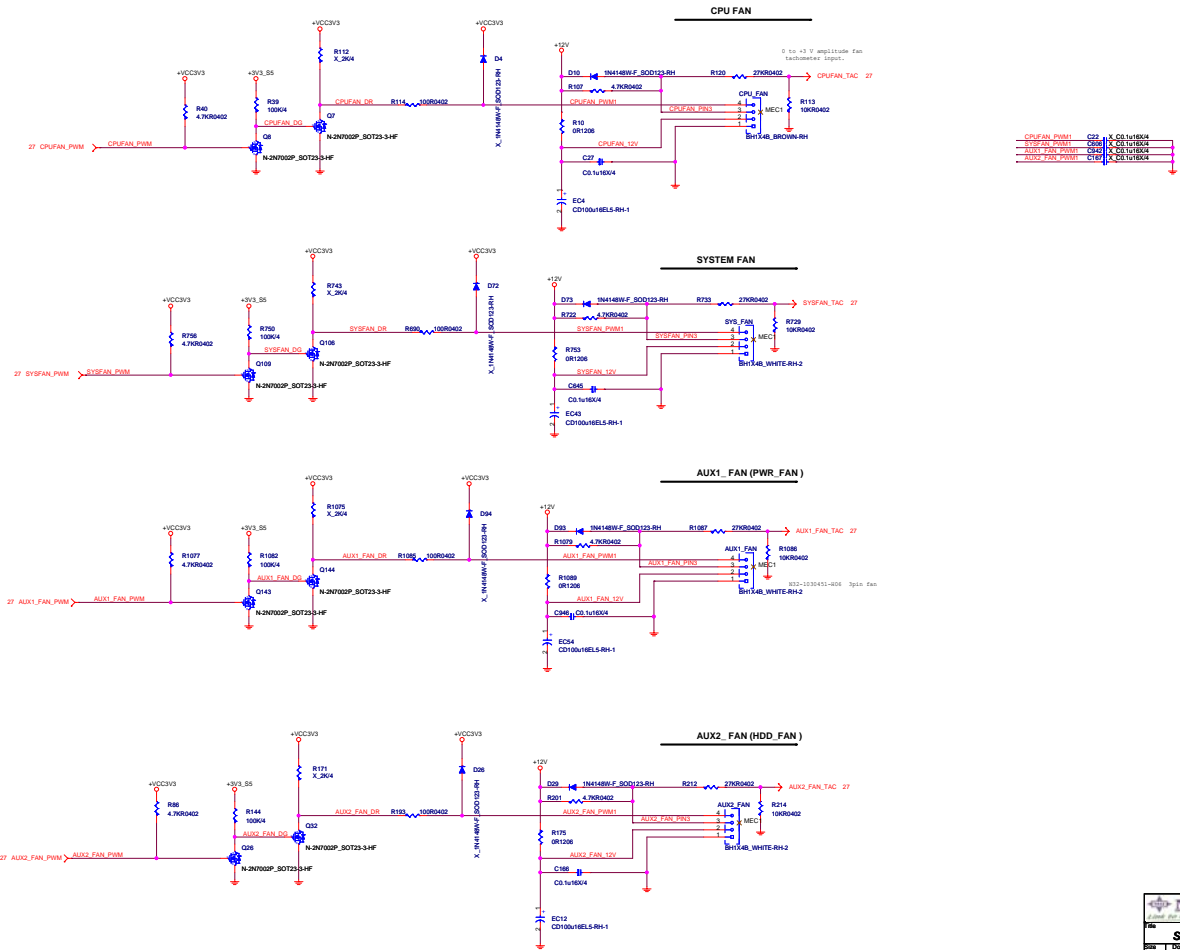
 <b>MSI</b> <small>THE MASTER OF QUALITY</small>				<a href="#">Link to the Future</a>				<b>MICRO-START INT'L CO.,LTD.</b>			
Title											
<b>PCI Slot</b>											
Size		Document Number							Rev		
		<b>MS-7C26</b>							<b>1.0</b>		
Date: Monday, May 27, 2019				Sheet		19		of		47	



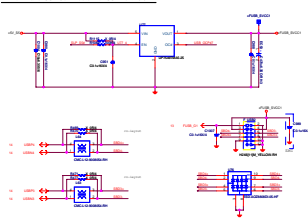




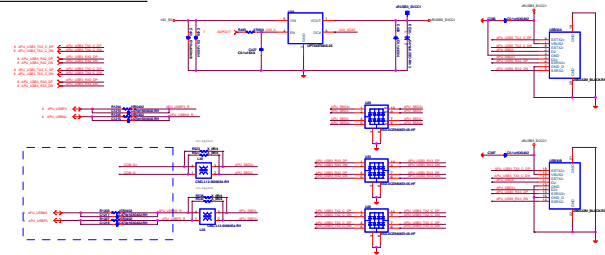
## CPU FAN /SYSTEM FAN /POWER FAN



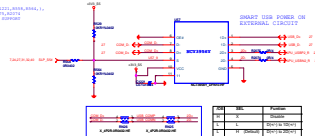
Front Panel USB Connector For USB Port 2/3



Rear Panel USB Connector For USB Port 3/4

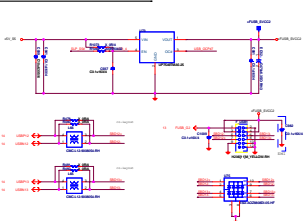


SWAP USB POWER ON  
EXTERNAL CONNECT

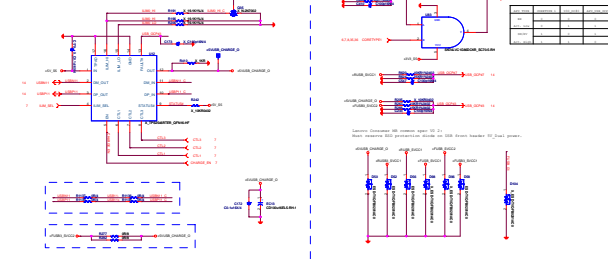


Pin	Signal	Function
1	NC	NC
2	NC	NC
3	NC	NC
4	NC	NC

Front Panel USB Connector For USB Port 1

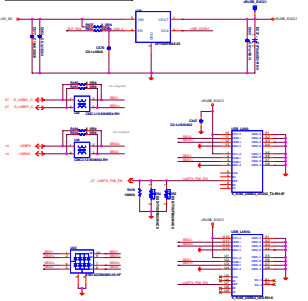


USB2.0 With Charge

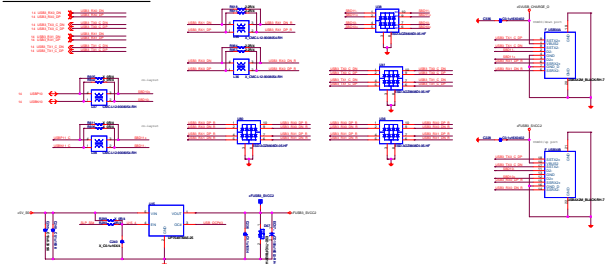


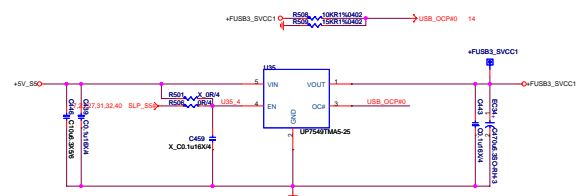
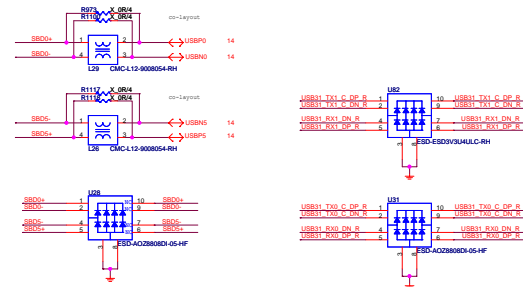
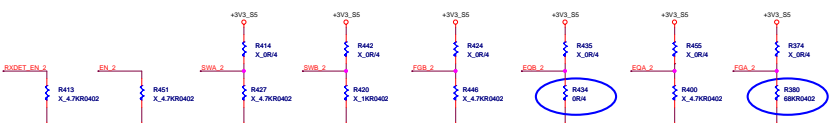
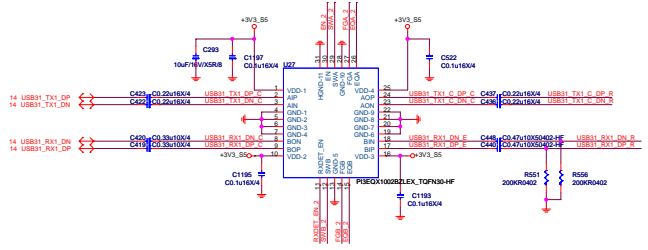
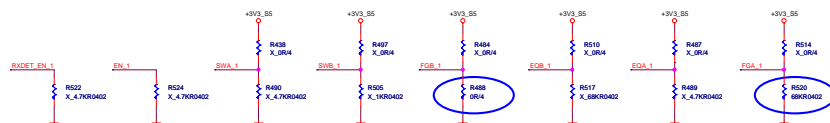
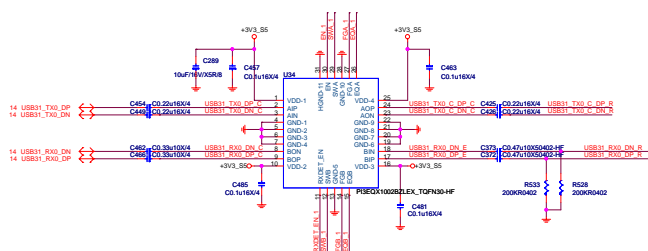
Pin	Signal	Function
1	NC	NC
2	NC	NC
3	NC	NC
4	NC	NC

Rear USB Connector For USB Port 1/4



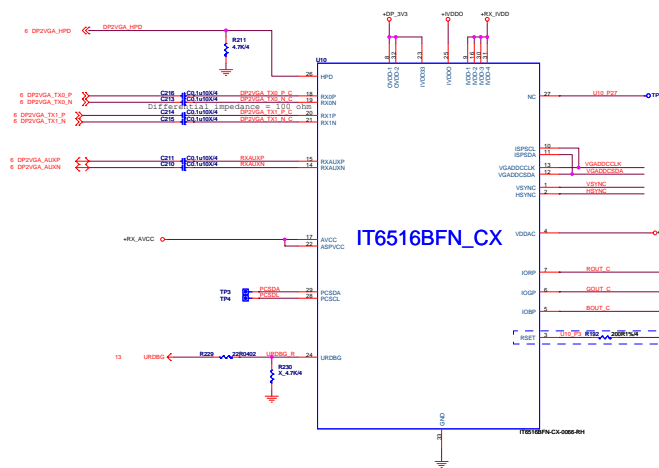
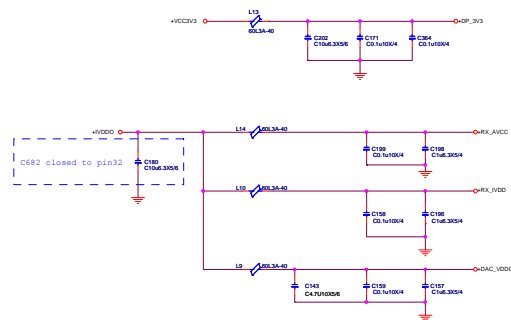
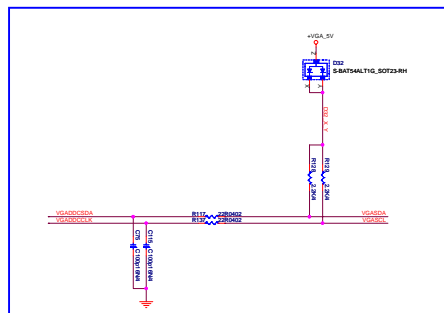
Front Panel USB Connector For USB Port 3/4



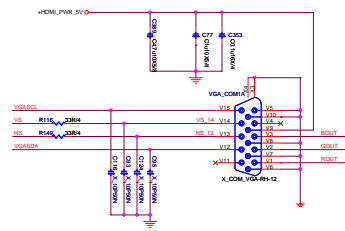
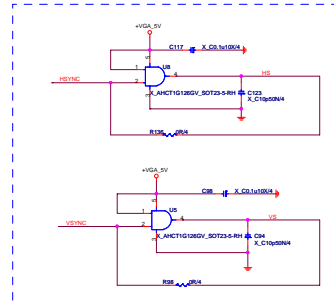
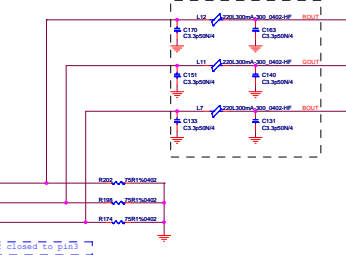
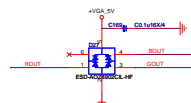
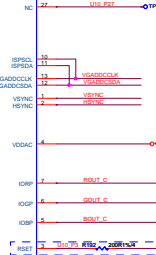


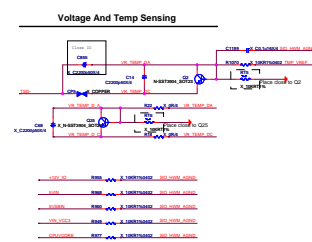
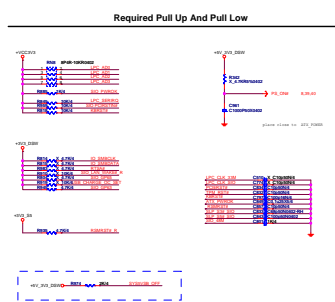
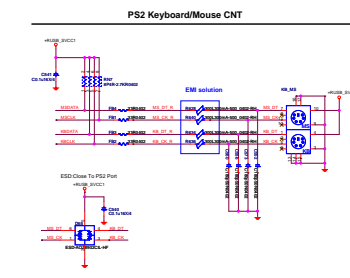
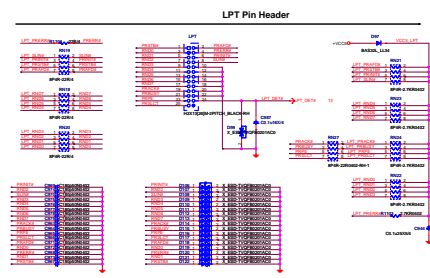
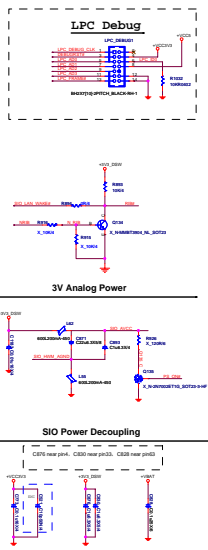
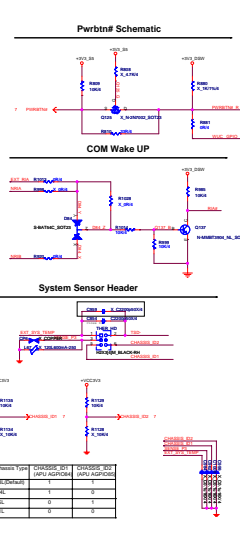
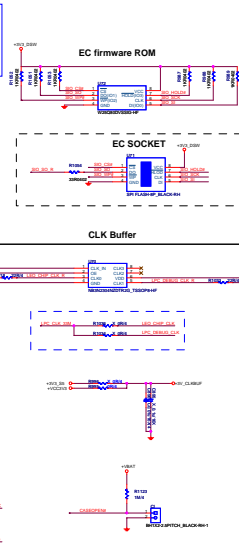




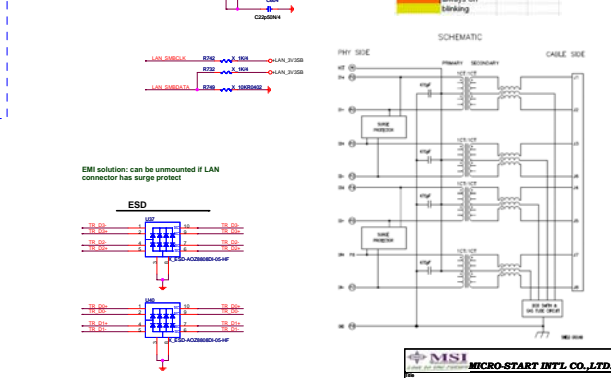
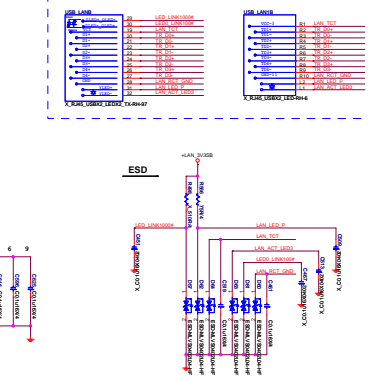
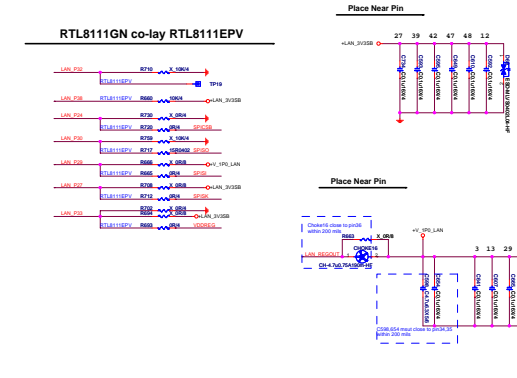
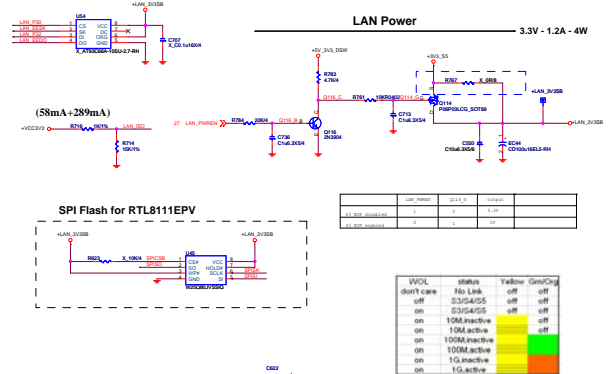
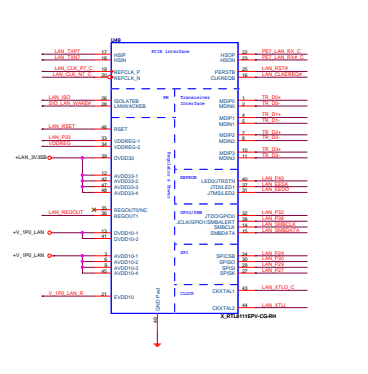
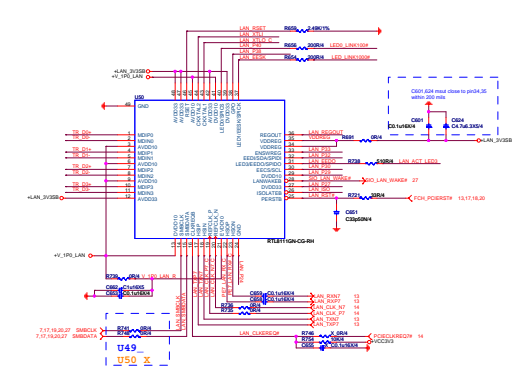


I6T516BFX\_CX

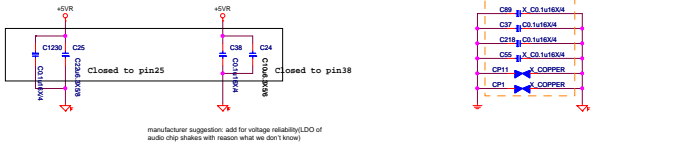
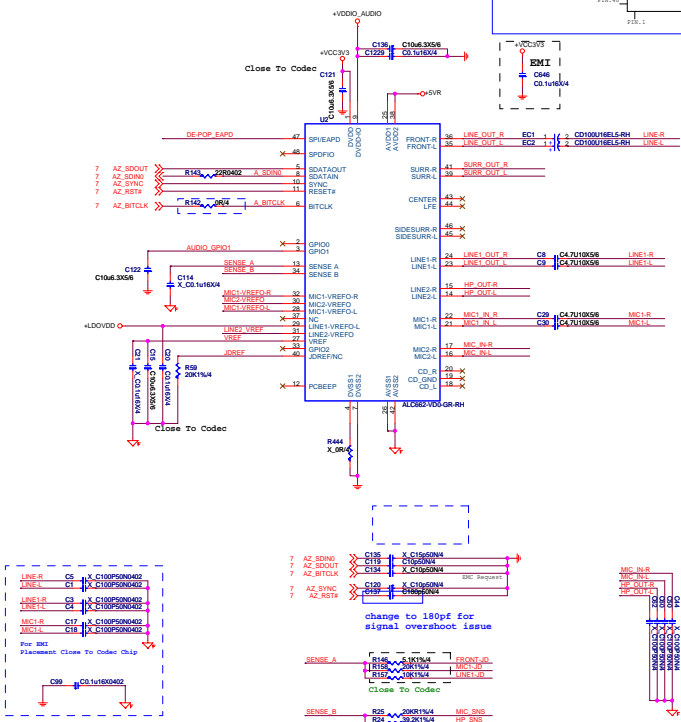
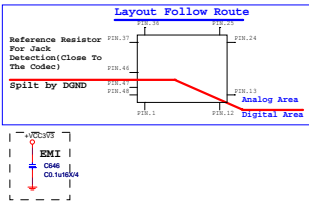




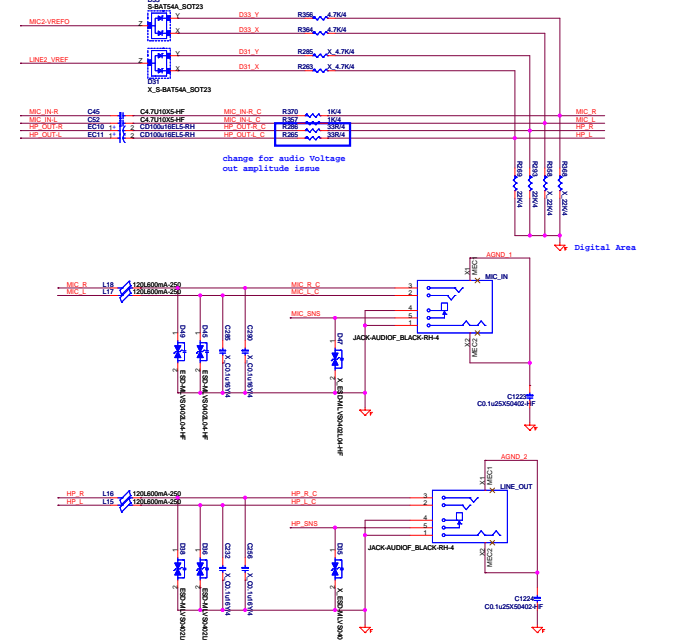
Gigabit LAN RTL8111GN co-layer RTL8111EPV



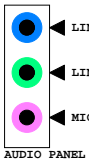
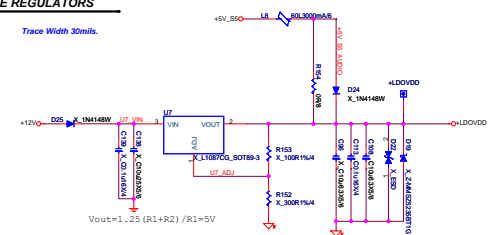
removed ALC662VC co-lay schematic on 0D



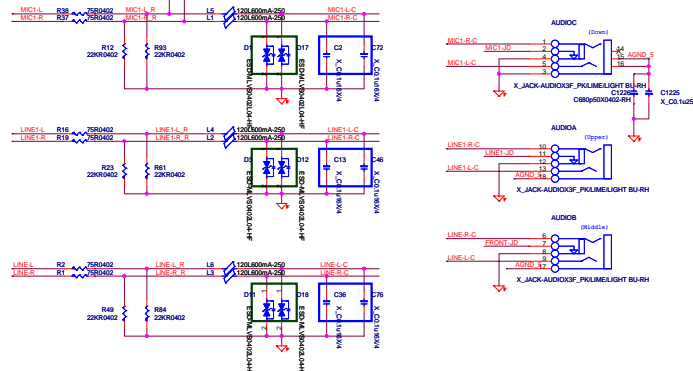
## EMC Request



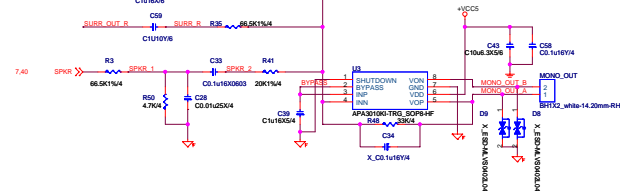
**Trace Width 30mils**



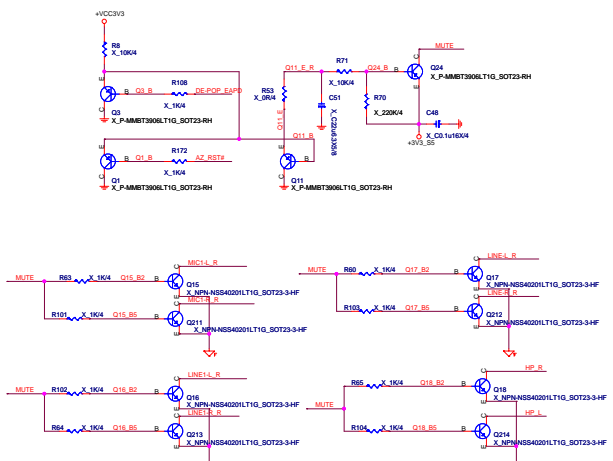
Lenovo EMC request



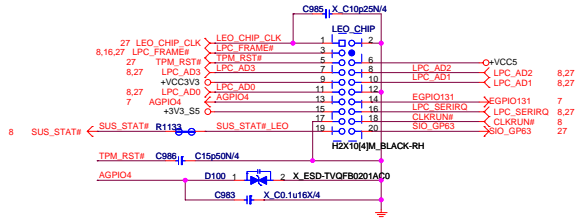
### MONO Amplifier



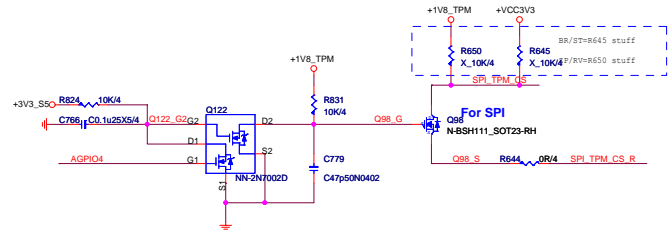
Audio DE BOB



## TCM Header

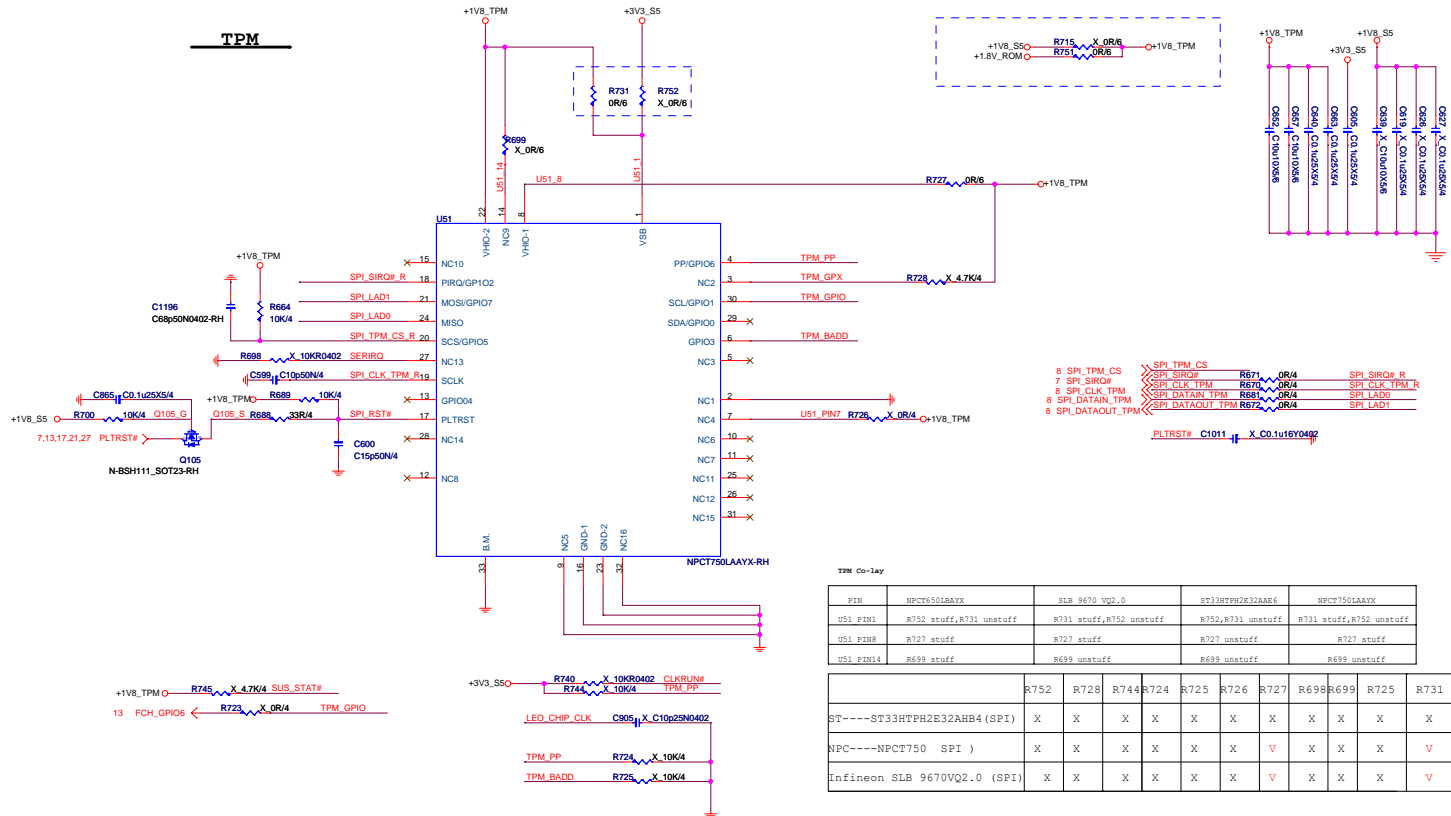


## TPM disable circuit



AGPIO4	HIGH	LOW
TPM	ENABLE	DISABLE

## TPM



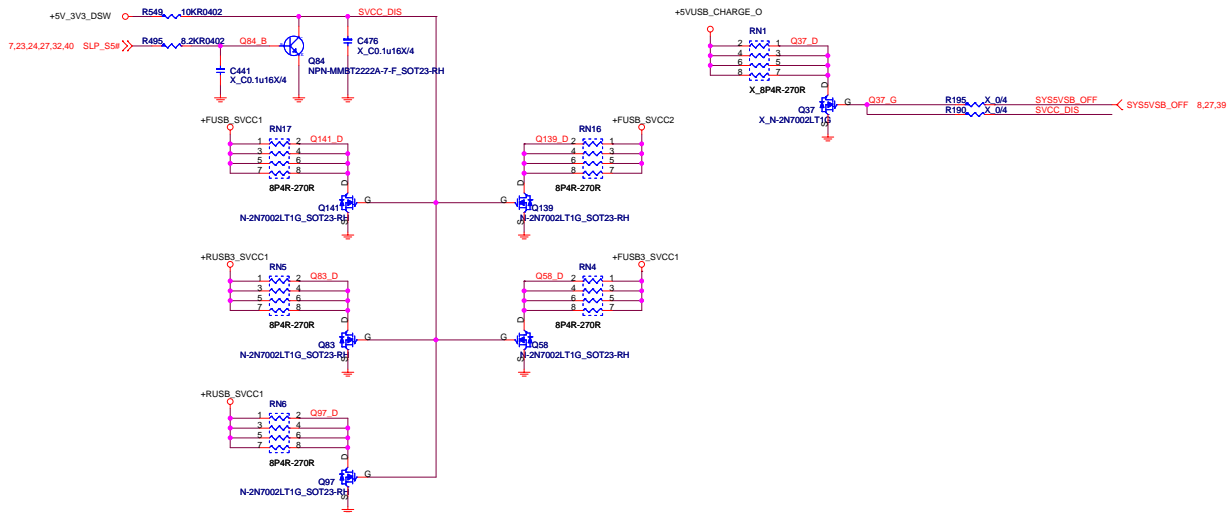
TPM Co-lay

Pin	NPCT7501AAYX	SLB 9670 VQ2.0	ST33HTPH2E32AA66	NPCT7501AAYX
U51 PIN1	R752 stuff, R731 unstuff	R731 stuff, R752 unstuff	R752, R731 unstuff	R731 stuff, R752 unstuff
U51 PIN8	R727 stuff	R727 unstuff	R727 stuff	R727 stuff
U51 PIN14	R699 stuff	R699 unstuff	R699 unstuff	R699 unstuff

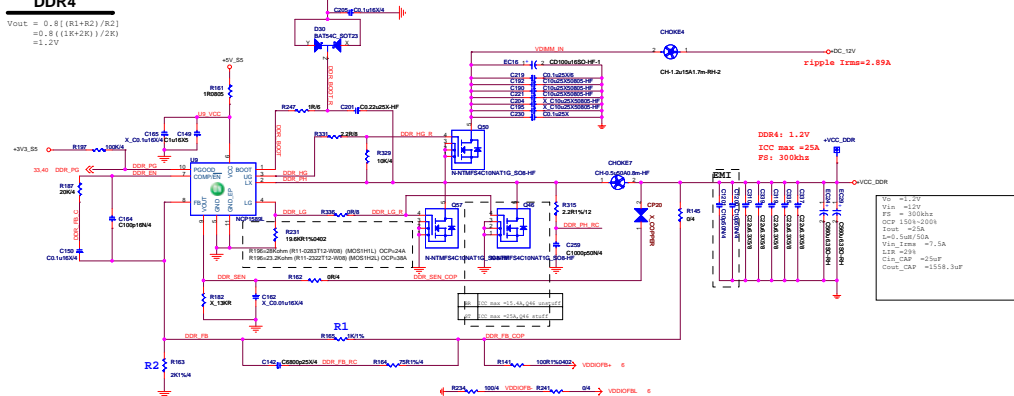
	R752	R728	R744	R724	R725	R726	R727	R698	R699	R725	R731
ST---ST33HTPH2E32AHB4 (SPI)	X	X	X	X	X	X	X	X	X	X	X
NPCT---NPCT7501 (SPI)	X	X	X	X	X	X	V	X	X	X	V
Infineon SLB 9670VQ2.0 (SPI)	X	X	X	X	X	X	V	X	X	X	V

## USB power discharge circuit



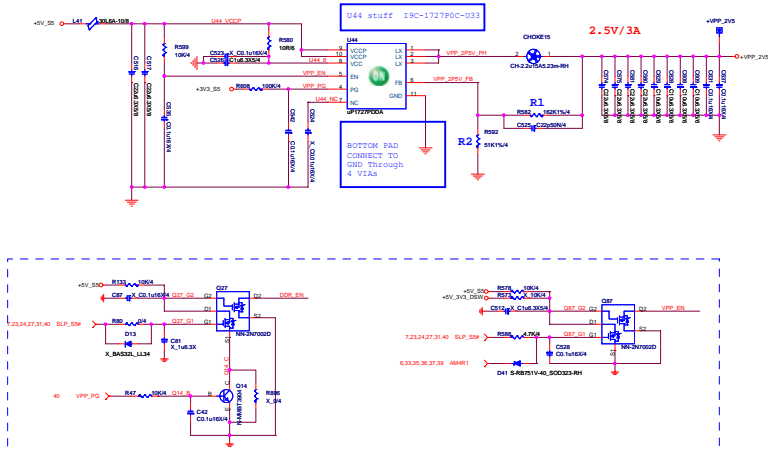
## DDR4

$$\begin{aligned} V_{out} &= 0.8[(R1+R2)/R2] \\ &= 0.8[(1K+2K)/2K] \\ &= 1.2V \end{aligned}$$

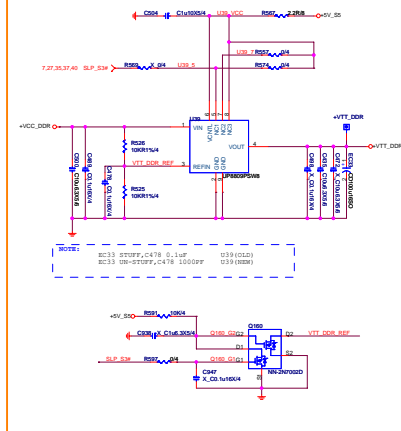


VPP\_2.5V

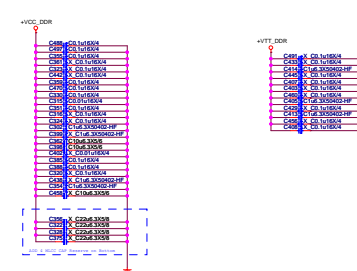
$$\begin{aligned} V_{out} &= 0.6[(R_1+R_2)/R_2] \\ &= 0.6[(10K+3.16K)/3.16K] \\ &= 2.5V \end{aligned}$$



**DDR4 Termination Power**  
0.6V - 1.1A - 0.825W



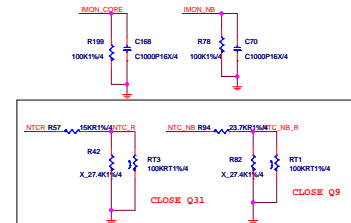
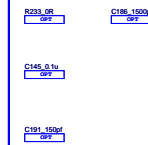
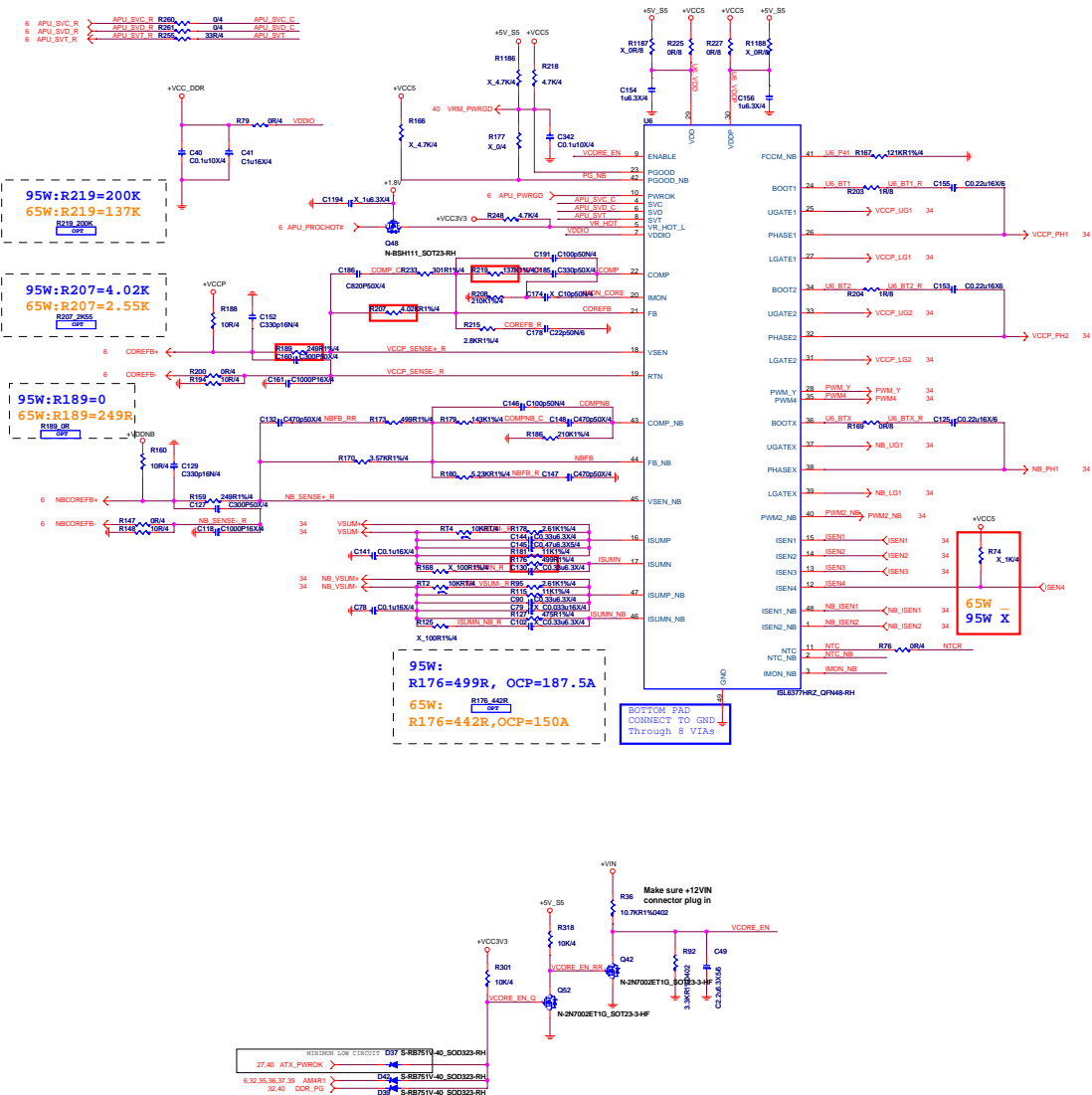
DDRIII I/O power decoupling caps.





ISL6377HRZ  
95W(A-Group) 4+2 Phase  
65W(C-Group) 3+2 Phase

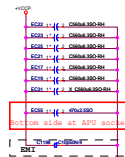
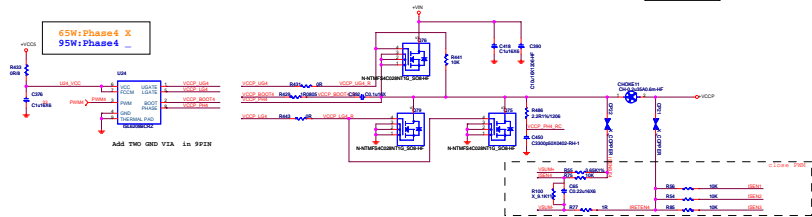
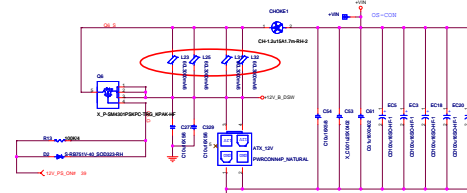
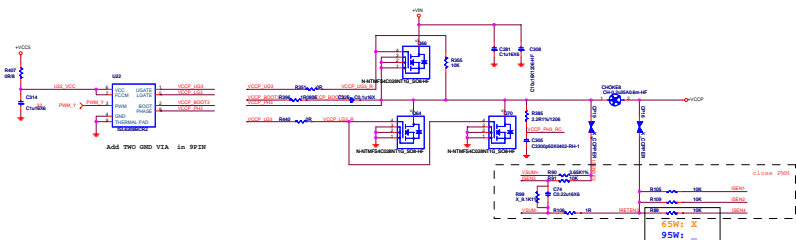
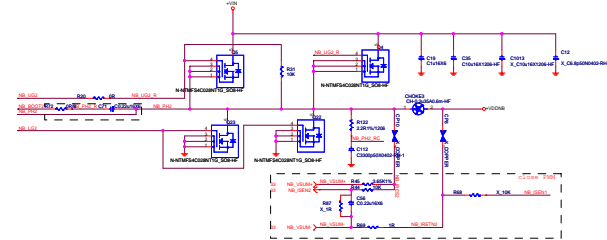
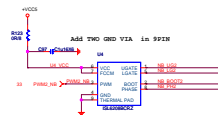
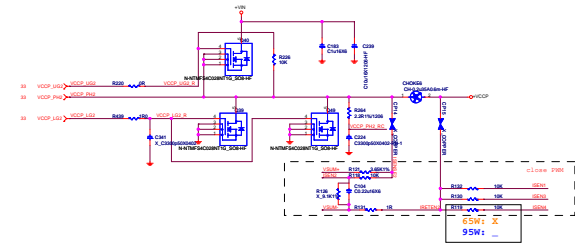
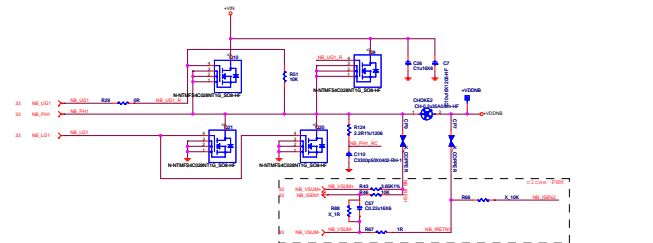
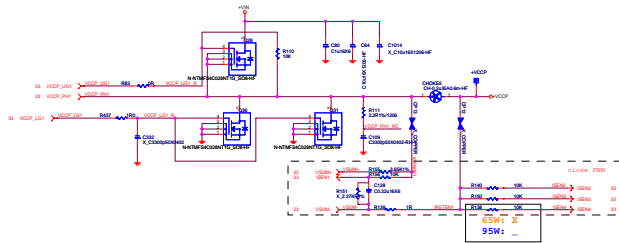
65W(SPECIAL)



OTP: R735 轉 隔位單孔

VCCP=0.75V-1.5V  
95W(A-Group) TDC:80A, EDC:125A  
65W(C-Group) TDC:65A, EDC:95A

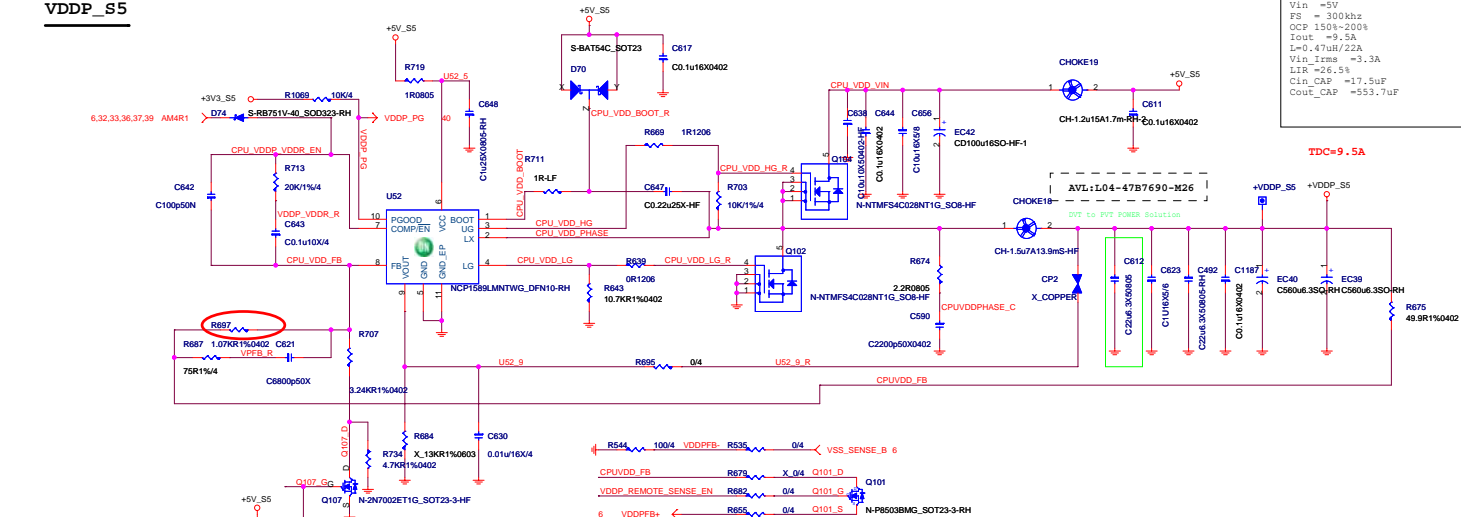
VCCP\_NB=0.75V-1.2V  
95W(A-Group) TDC:30A, EDC:35A  
65W(C-Group) TDC:50A, EDC:75A



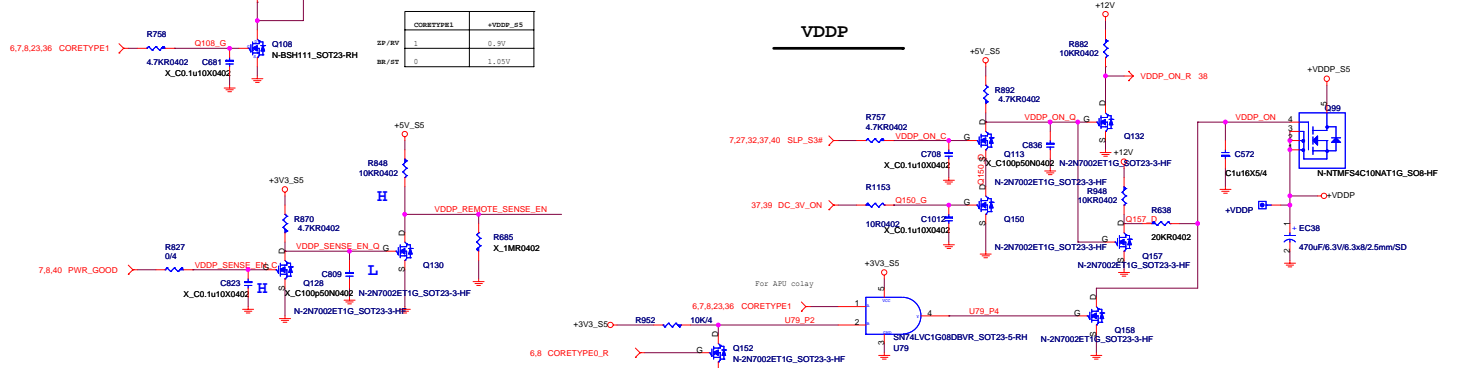
# VDDP\_S5

Vo = 1.05V  
VIn = +5V  
FS = 300kHz  
OCP 150%~200%  
Iout = 9.5A  
I=0.47uH/22A  
VIn\_Irms = 3.3A  
LIR = 26.5%  
CIn\_CAP = 17.5uF  
Cout\_CAP = 553.7uF

TDC=9.5A



## VDDP

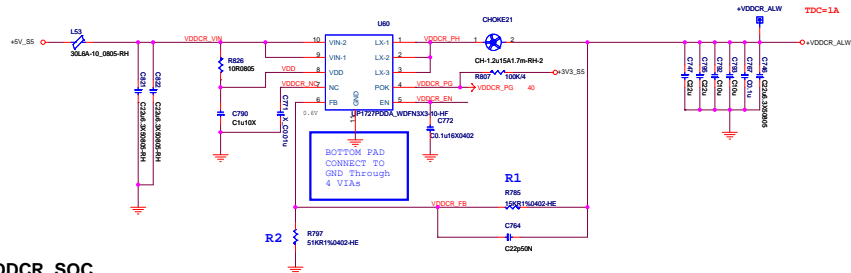


For APU relay

PIN	CORETYPE1	CORETYPE0	U79_P2	U79_P4	+VDDP
Type 0	0	0	1	0	High
Type 2	1	0	1	1	Low
Type 3	1	1	0	0	High

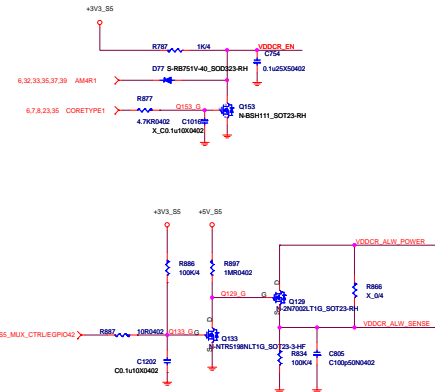
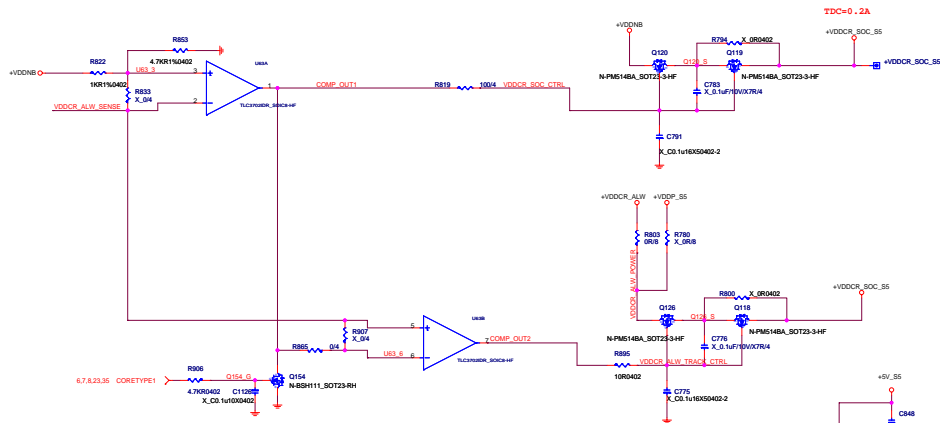
**MSI**  
**MICRO-START INT'L CO.,LTD.**  
**VDDP/VDDP\_S5**  
 Document Number  
**MS-7C26**  
 Date: Monday, May 27, 2019 Sheet 35 of 47

## VDDCR\_ALW



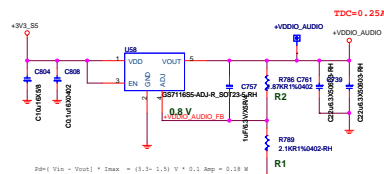
$V_o = 0.775V$   
 $V_{in} = 5V$   
 $F_S = 1000kHz$   
 $Current\ limit = 5-6A$   
 $I_{out} = 1A$   
 $L = 1.1\mu H/27A$   
 $V_{in\_Tmax} = 0.35A$   
 $LIR = 40\%$   
 $C_{in\_CAP} = 0.43\mu F$   
 $C_{out\_CAP} = 11\mu F$

## VDDCR\_SOC



State	s5_mux_ctrl1	s3#	s5#	VDDCR_SOC_S5 Voltage
G3	X	0	0	OFF
S5	0	0	0	ON(=+VDDCR_ALW)
S3	0	0	1	ON(=+VDDCR_ALW)
s0,but still in Reset	0	1	1	ON(=+VDDCR_ALW) or if VDDNB>+VDDCR_ALW, Tracks VDDNB
S0	1	1	1	Tracks +VDDNB

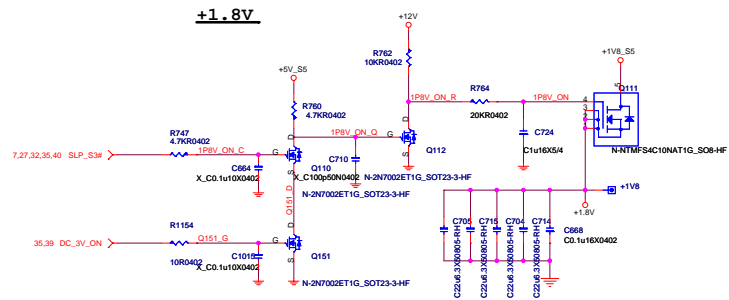
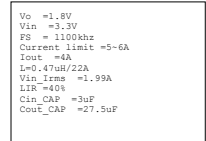
## +VDDIO\_AUDIO Nominal Vout=1.50V



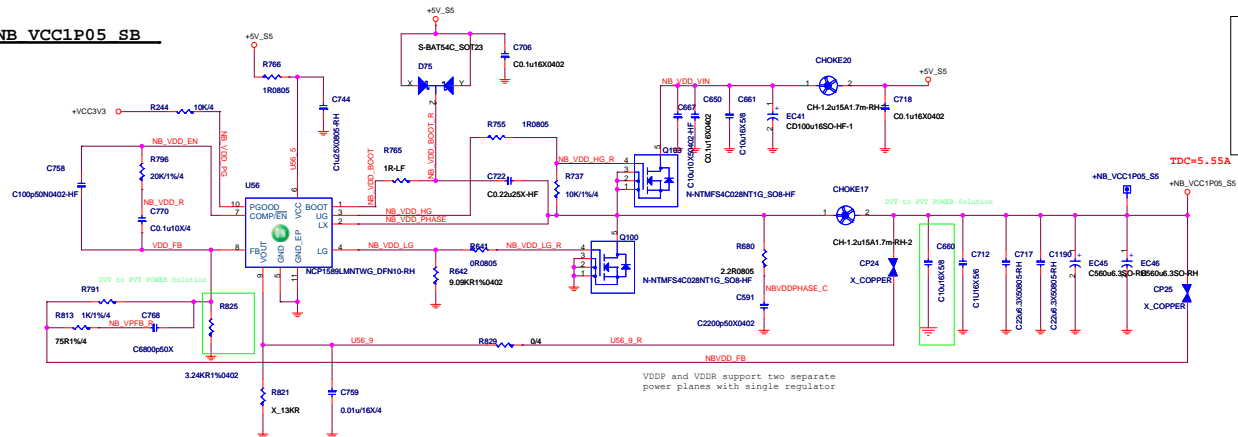
$$P_{in} = (V_{in} - V_{out}) \times I_{max} = (5.3 - 1.5) V \times 0.1 A = 0.38 W$$

$$V_o = 0.8 \times (R1 + R2) / R1$$

**+1.8v & +1.8v\_S5**



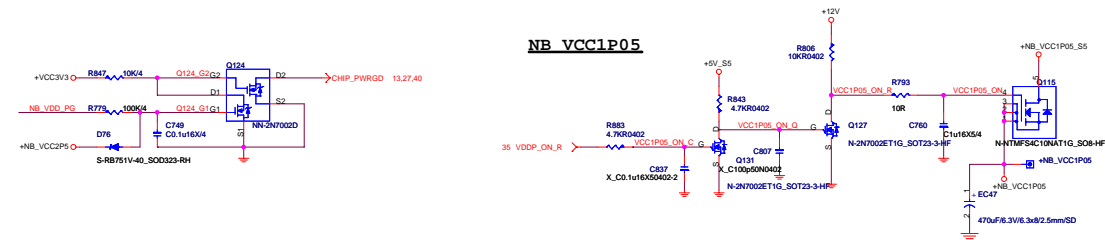
NB VCC1P05 SB



```
Vo =1.05V
Vin =5V
FS = 300khz
OCP 150%-200%
Iout =5.55A
L=1.1uH/27A
Vin_Irms =2.26A
LIR=45%
Cin_CAP =10.2uF
Cout_CAP =223.3uF
```

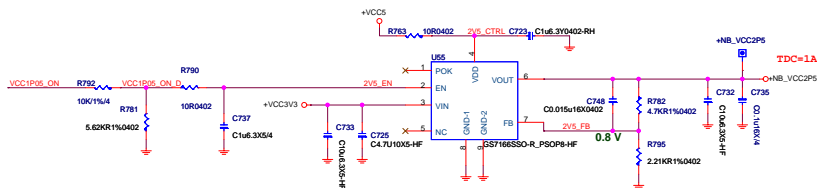
VDDP and VDDR support two separate power planes with single regulator

NB VCC1P05



NB VCCP2P5

$$\begin{aligned} V_{out} &= 0.8[(R_1+R_2)/R_2] \\ &= 0.8((4.7K+2.21K)/2.21K) \\ &= 2.5V \end{aligned}$$



5V  
19.5A

5V  
19.5A

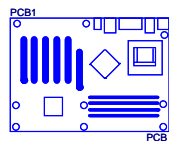
5V  
19.5A



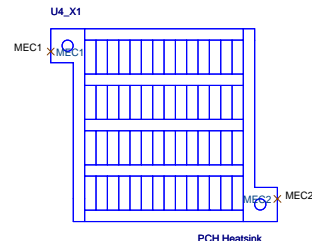
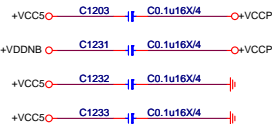




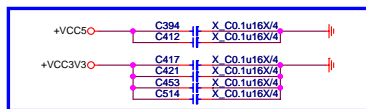
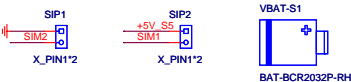
## Manual Parts



### For AMD



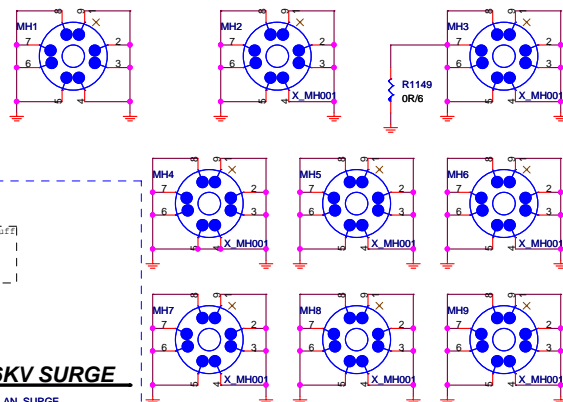
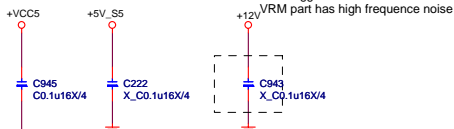
## Simulation



## Mounting Holes

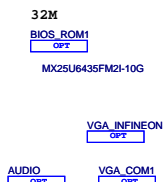


## For EMI



## Optics Orientation Holes

### Optical Fiducial Marks-120



### Without SURGE

### With 6KV SURGE

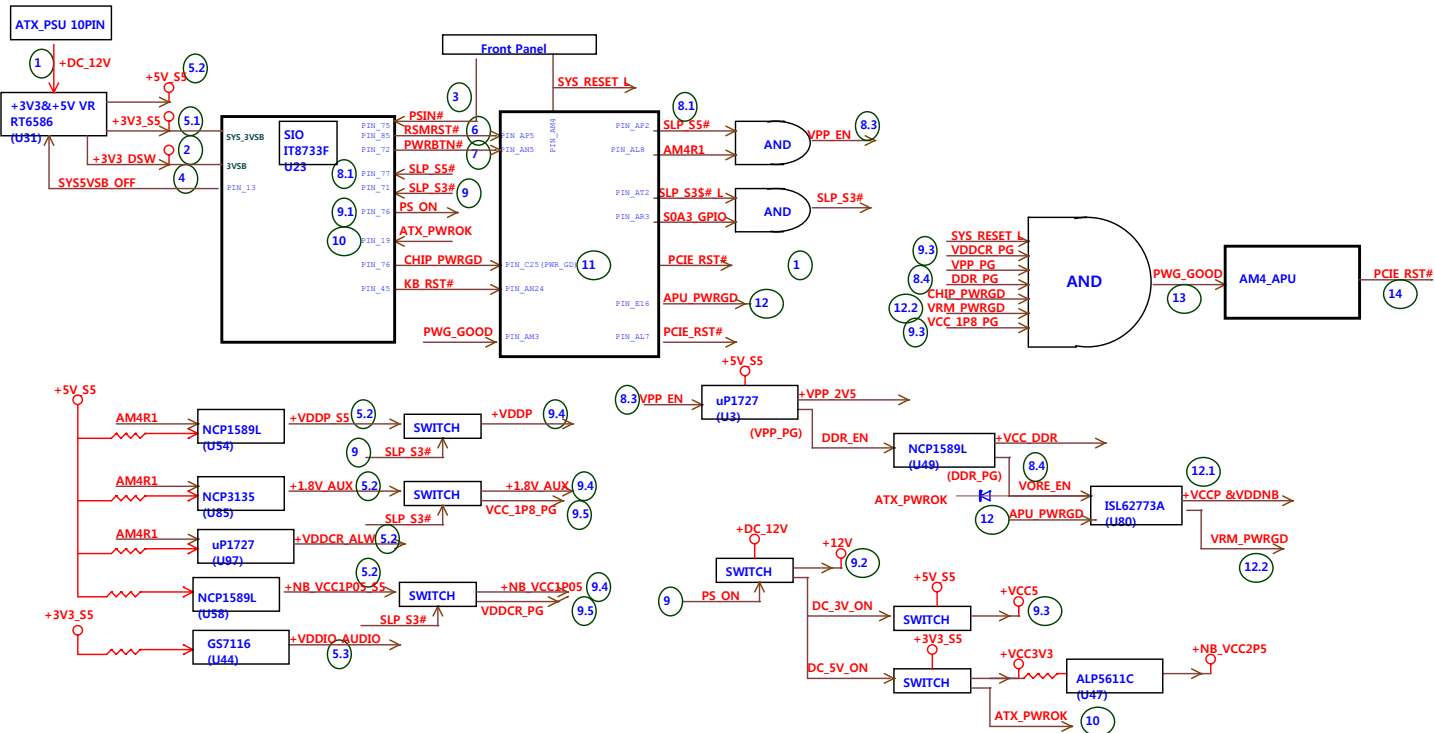
### Reserve with surge single LED



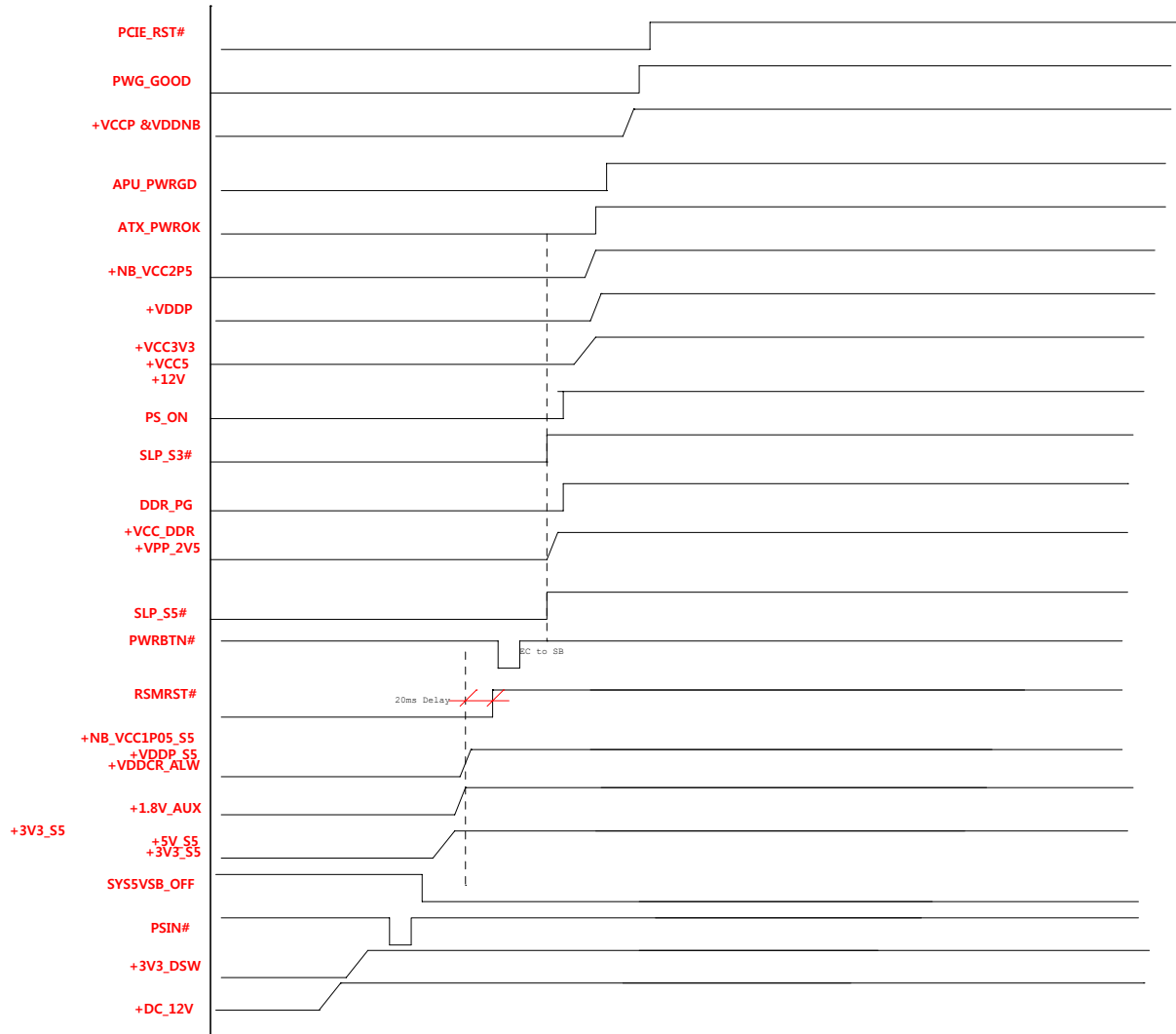
<b>MICRO-START INTL CO.,LTD</b>		
Title <b>Manual &amp; Option Parts</b>		
Size	Document Number	Rev
	<b>MS-7C26</b>	<b>1.0</b>
Date:	Wednesday, May 29, 2019	Sheet 41 of 47



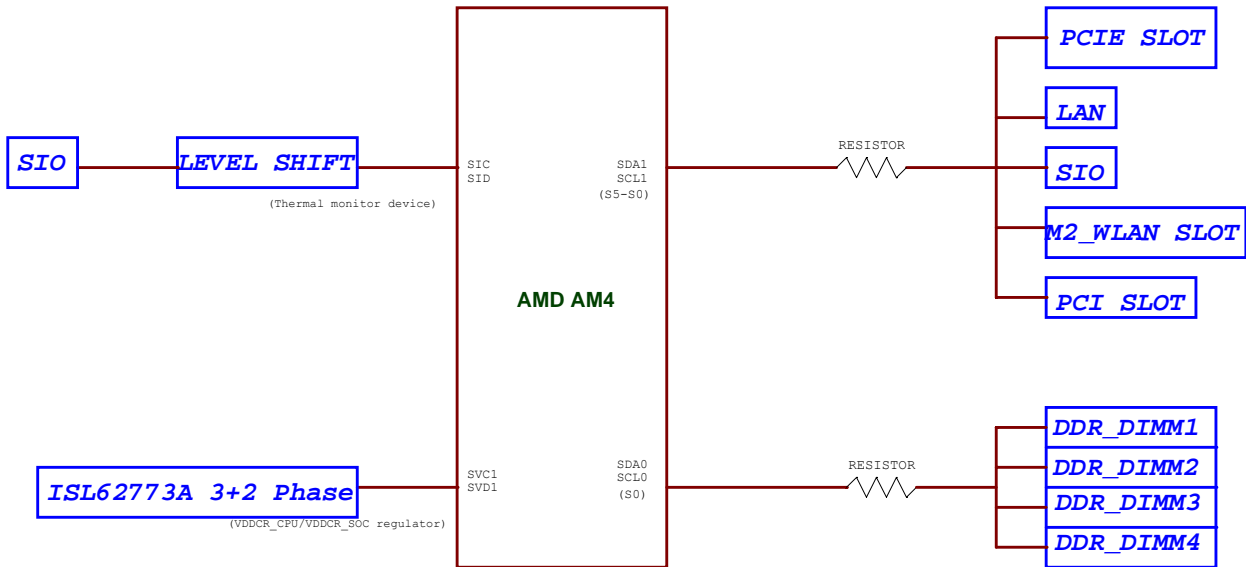
### Power Sequence Diagram



## Power Sequence Timings







# RESET MAP

